Design of Operational Transconductance Amplifiers for Voltage to Current Conversion in Gas Sensing Applications

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***Abstract*— This paper presents a study of Operational Transconductance Amplifiers (OTAs) for voltage to current conversion circuits. The paper includes a comparative analysis of three OTA architectures implemented in 0.35µm CMOS AMS Technology under ± 1.65V power supply voltage. The impact of the OTA topology has been investigated by simulation. The designed OTAs managed to deliver large current values of 10mA and 1mA to the load with a worst-case error of 0.02% under worst-case power supply and temperature conditions and a worst percentage error of 0.12% under process variation for both Miller Compensated and Capacitor Multiplier Compensated OTA.**

Keywords—voltage to current conversion;two stage compensated Miller OTA; two stage compensated Capacitor Multiplier OTA; Rail-to-Rail Folded Cascode OTA; resistive gas sensors

I. INTRODUCTION

Voltage-to-current converters (V–I) also named as current regulators or current sources are considered basic building blocks in several applications like continuous-time filters, data converters and interface circuits. Usually high linearity of the V–to-I conversion over a large input range is required for these applications [1].

The current regulator utilizes an operational amplifier (op amp) or an Operational Transconductance Amplifier (OTA) and a transistor to provide a voltage to the resistor R. A reference voltage, which can be provided by a band gap reference, is applied to the non-inverting input of the op amp. If the op amp operation is close to ideal, then the voltage at the inverting input will be equal to the reference voltage.

The current regulator shown in Fig.1 locks the output voltage to the reference input voltage V_{ref} by an amplifier and a resistor. The voltage across the resistor R_{sens} will be fixed to the voltage difference across R_{sens} that is equal to V_{ref}-V_{ss} in case of Fig.1.a [1], [2]. On the other hand, the voltage across the resistor can be bounded between two voltage references V_1 and V_2 like in the case of Fig.1.b [3], [4]. The resulted voltage across the R_{sens} in this case is V_1-V_2. Therefore, the voltage across R_{sens} is fixed and the variation of the resistance is converted into a variation of current.

Resistive gas sensors are also known as chemo-resistive sensors. In the presence of targeted analyte, such sensors have the role to convert the chemical changes about the concentration of the gas in the atmosphere into an electrical signal in the form of a variation of resistance. The sensors resistance R_{sens} varies across several decades [5]. An accurate voltage to current conversion is required to fix the voltage across the sensor, so that, the variation of the resistance is changed into a current signal guaranteeing an accurate sensing operation.

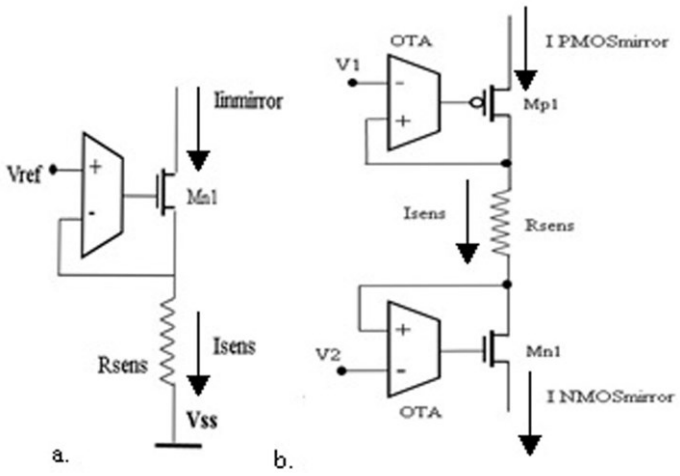

Fig.1. Voltage to current conversion circuits architectures

The paper presents the design of three different Operational Transconductance Amplifiers (OTAs) topologies used in the feedback amplifier of the voltage reference. The performance analysis of these OTAs under typical and worst case temperature and power supply i.e. 80^0C and ±1.5V is demonstrated. For the configuration presented in Fig.1.a the percentage error of the voltage required to be fixed across the variable resistance R_{sens} is measured as well.

The paper is organized as follows. Section II presents the amplifier requirements and state of the art to obtain high accurate voltage to current conversion. In Section III, the design of three different OTA topologies is presented, while their full comparison and the results are drawn in Section IV. Section V concludes the paper.

II. AMPLIFIER DESIGN REQUIREMENTS AND STATE OF THE ART

The most effective way to convert a voltage signal into a current is to use a feedback OTA whose input is connected to a reference voltage. The reference voltage will be imposed across the resistor and the output current in this case is the same as the one of the resistor. In order to deliver large current to the load the OTA has also to be designed having two stages where the first stage is the OTA and the second one is the source follower stage [6].

For resistive gas sensing applications, the resistance of the sensor ranges across several decades. The OTA requires to be high gain (≈100dB), low bandwidth (tens of Hz), low noise OTA and the output stage is a source follower in order to deliver the high current to the load especially when R_{sens} is small i.e. the current is in (mA) according to [2].

In this paper, for the proposed application where R_{sens} varies from 100Ω to 1GΩ, we present the design of three different OTA topologies, the two stage Miller Compensated OTA (MCO), the two stage Capacitor Multiplier Compensated OTA (CMCO) and the one stage Rail-to-Rail Folded Cascode OTA (RRFCO). The performance of the three topologies is analyzed under both typical conditions and worst-case power supply voltage (±1.5V) and temperature (80^0C) conditions. For the three designed topologies, the current regulator achieved high accuracy in fixing the voltage across the resistance of the sensor. The corner simulations are also considered and presented to ensure a robust design. Simulation results shows that the current regulator with two stage MCO is being less affected by environmental and process variations.

III. AMPLIFIER DESIGN

In this section, we present the design of three different Operational Transconductance Amplifiers (OTAs) used in the current regulator analog circuit to fix the voltage accurately across the resistance of the sensor for gas sensing applications. The design includes two stage Miller Compensated OTA, two stage Capacitor Multiplier Compensated OTA, and Rail-to-Rail Folded Cascode OTA. The three different topologies were designed in 0.35µm CMOS Technology under 3.3V supply voltage. In order to reduce the Flicker noise PMOS differential pair is used in the input stage for the first two designed topologies.

A. Two-Stage Miller Compensated OTA

The topology of two stage Miller compensated OTA is shown in Fig.2. The first stage has the role to convert the voltage input into a current whereas the second stage increases the gain of the OTA due to the high output resistance provided by r_{06} in parallel with r_{07}, where r_{0i} is the channel resistor of the transistor. The compensation capacitor C_c is placed between the input and the output of the second stage, so that, to split the poles into two sides one pole placed at lower frequencies and the other is moved to high frequencies. The compensation capacitance used for this OTA is 20pF. The simulated performance is summarized in TABLE.I, TABLE.II, and TABLE.III.

B. Two-Stage Capacitor Multiplier Compensated OTA

The topology of two stage Capacitor Multiplier Compensation OTA is shown in Fig.3. The first stage of this OTA, which is named as capacitor multiplier stage, blocks the feed forward capacitive path from the output of the first stage to the output of the amplifier. In this case, the right half zero is removed whereas, the left half zero is introduced. The latter boosts the phase margin and improves the stability of the OTA [7]. The amplifying stage is realized by a transconductance stage as in usual CMOS technologies. The Capacitor Multiplier permits the amplifier to drive very large capacitive load using a small compensation capacitor. The compensation capacitance C_c used in this topology is only 0.9pF and R_c is equal to 60kΩ. The simulated performance is summarized in TABLE.I, TABLE.II, and TABLE.III.

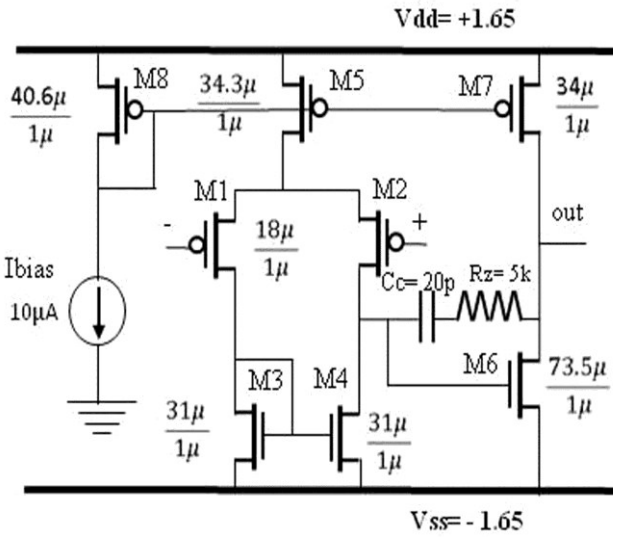

Fig.2. Two Stage Miller Compensated OTA Topology

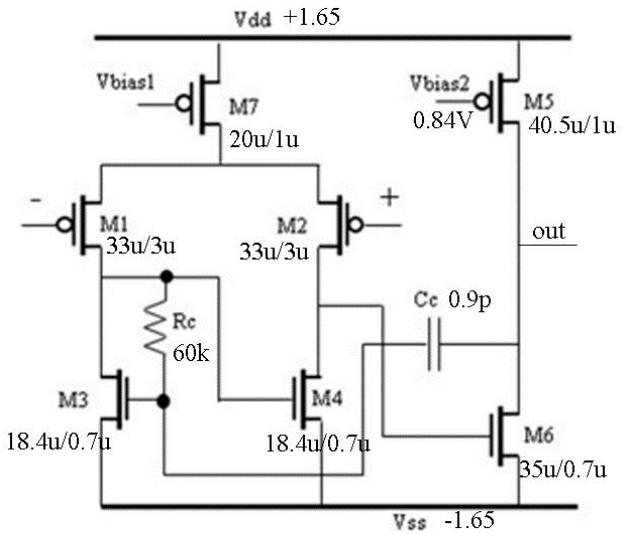

Fig.3. Two- stage Capacitor Multiplier Compenssated OTA

C. One-Stage Rail- to-Rail Folded Cascode OTA

An OTA with Rail-to-Rail input swing achieves high linearity over large input range, and is insensitive to the transistors non-idealities like geometric or parametric mismatches [1]. Rail-to-rail input techniques mainly revolve around the idea of maintaining a constant input transconductance (gm) across the full common-mode range. Fig. 4 shows a Rail to Rail Folded Cascode Topology used in the design of the current regulator. The folded cascode is generally compensated by the load capacitance thus; there is no need for an additional compensation and a second stage. Using the Rail-to-Rail input, the current mirroring output will not cause a reduction in the voltage to current operating range. The simulated performance is summarized in TABLE.I, TABLE.II, and TABLE.III.

IV. RESULTS

In order to check the accuracy of the converted current as well as the performance of the designed OTAs, the OTA circuit topologies presented in section III were designed in 3.3V-0.35µm, N-WELL, four metal AMS CMOS technology where the threshold voltages for NMOS and PMOS transistors are 0.5V and 0.7V respectively. The functionality of these circuits is simulated in PSPICE OrCAD CAD tool. The geometric sizing of the designed OTAs which are the MCO, CMCO and RRFCO is shown in Fig.2, Fig.3, and Fig.4 respectively. TABLE. I and TABLE.II represent the performance analysis of the three designed OTAs considering the DC Gain, bandwidth BW, Gain Bandwidth GBW, phase margin PM, common mode rejection ratio CMRR, power supply rejection ratio PSRR, power dissipation, and the input common mode range ICMR. The performance of the OTAs is also analyzed under typical and worst case to ensure the robustness of the proposed design. For identical power supply and output, the three OTAs were designed to have a high DC gain and low bandwidth (BW) as reported in [2]. The results presented in TABLE.I show that high DC gain and low bandwidth is obtained when Capacitor Multiplier Compensation is used. However, the Miller Compensated OTA is found to be less affected by environmental variables under worst-case temperature and power supply as well as process variations, as shown in TABLE.II and TABLE.III. Note that FF corresponds to fast PMOS fast NMOS, FS for fast PMOS slow NMOS, SF for slow PMOS fast NMOS and SS for slow PMOS slow NMOS. Whereas, the one stage Rail-to-Rail Folded Cascode OTA is

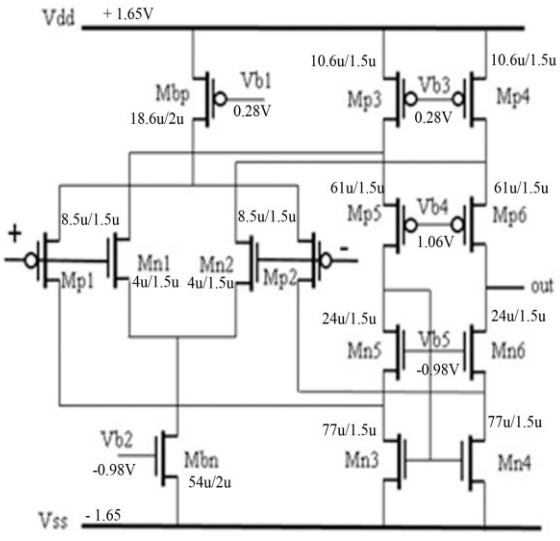

Fig.4. One Stage Rail-to –Rail Folded Cascode OTA

TABLE .I. PERFORMANCE ANALYSIS OF THE THREE DESIGNED OTAS UNDER TYPICAL CASE

	Miller Compensation	**Capacitor Multiplier Compensation**	**Rail to Rail Folded Cascode**
DC Gain	96.8dB	117.6dB	91.6dB
BW	12.6Hz	2.71Hz	5.6Hz
GBW	957kHz	2.35MHz	163.8kHz
PM	113.6^0	120^0	54^0
CMRR	102.4dB	115.7dB	120.6dB
PSRR+	65dB	44.4dB	6.26dB
PSRR-	99.3dB	104.55dB	5.67dB
Power dissipation	129.8µW	82.1µW	43.8µW
ICMR	(-1.6 to 1.4)	(-1.6 to 1.33)	(-1.5 to 1.5)

TABLE .II. OTAS UNDER WORST CASE TEMPERATURE AND POWER SUPPLY (80^0C AND 3V).

	Miller compensation	**Capacitor Multiplier Compensation**	**Rail to Rail folded Cascode**
DC Gain	95.7dB	101.4dB	61.6dB
BW	13.2Hz	18.34Hz	113Hz
GBW	858.6kHz	2.5MHz	124.8kHz
PM	109^0	121^0	75.2^0
CMRR	101.1dB	142.2dB	101.9dB
PSRR+	68dB	28.5dB	54.56dB
PSRR-	99dB	112.84dB	5.57dB
Power dissipation	117.9µW	75.735µW	10.76µW

TABLE .III. PERFORMANCE ANALYSIS OF THE THREE DESIGNED OTAS UNDER PROCESS VARIATIONS

	MCO				CMCO				RRFCO			
	FF	**FS**	**SF**	**SS**	**FF**	**FS**	**SF**	**SS**	**FF**	**FS**	**SF**	**SS**
DC Gain (dB)	100.5	103.4	98.3	100.24	97.5	97.5	117	102	53.2	57	72	74.6
BW (Hz)	5.5	4	6	4.9	36	42.7	3.3	21.75	15.4k	8.4k	1	6.23
GBW (Hz)	594k	593k	504k	502.5k	3.4M	4.4M	2.8M	3.5M	896k	5.6M	1.7k	29K
PM	89^0	92^0	90^0	92^0	127^0	135^0	122^0	128^0	21^0	76^0	27^0	70^0

TABLE.IV. %ERROR OF VSENS OF THE VOLTAGE TO CURRENT CONVERSION CIRCUIT UNDER TYPICAL CASE FOR THE THREE DESIGNED OTA TOPOLOGIES

Rsens (Ω)	**100**	**1k**	**10k**	**100 k**	**1M**	**10M**	**100 M**	**1G**
MCO	0.01	0.01	0.01	0.01	0.01	0	0	0
CMCO	0	0	0	0	0	0	0	0
RRFCO	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02

shown to be the topology mostly affected by the environmental and process variations.

To test the accuracy of the voltage across the variable resistance R_{sens} of Fig.1.a, the percentage error in the voltage to be fixed across R_{sens} is computed. The ideal voltage is taken according to equation 1.

$$V_{sens} = V_{ref} - V_{ss} \quad (1)$$

Where, the reference voltage is considered as -0.65V and Vss = -1.65V leading to a value of 1V fixed across R_{sens}.
Because there is no current going into the inverting input of a high input impedance op amp, then the current flowing through the resistor will also be the drain current of the transistor. So, this current source produces an output current based on the resistor value and the reference voltage, such that:

$$I_{sens} = \frac{V_{ref} - V_{ss}}{R_{sens}} \quad (2)$$

Fixing 1V across the sensor's resistance for a range of 100Ω to 1GΩ leads to a variation of current between 10mA to 1nA.

The percentage error of the voltage obtained by simulation ($V_{simulation}$) across R_{sens} taken the ideal voltage 1V as a reference is given by equation (3).

$$\%error = \frac{V_{sens} - V_{simulation}}{V_{sens}} \times 100 \quad (3)$$

TABLE. IV shows the percentage error of V_{sens} for the three designed OTAs under typical case. Regardless from using a source follower output stage the three topologies, achieve a worst percentage error of 0.02% corresponding to the Rail-to-Rail Folded Cascode OTA architecture and a best percentage error of zero for the capacitor multiplier OTA.

The current regulator was also tested under environmental corners considering the worst-case temperature and voltage supply, as well as, the process variations. Fig.5 represents the bar graph of the percentage error under the worst-case conditions for the three OTA topologies. The graph also shows that for one stage OTA the worst-case percentage error of the voltage is higher than the two stage OTAs. Fig.6 represents the maximum obtained percentage error along the full resistance range under process variations. The histogram assures that the accuracy of the one stage RRFCO is mostly affected by the process variations. This is because a second stage is required to support the large current (in the order of mA) to the load. Whereas, for

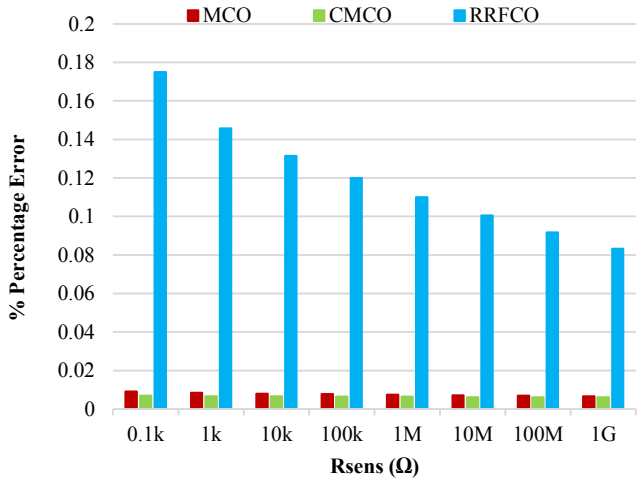

Fig.5. % error of the voltage obtained across the variable resistance Rsens for the three designed OTA topologies under worst case conditions.

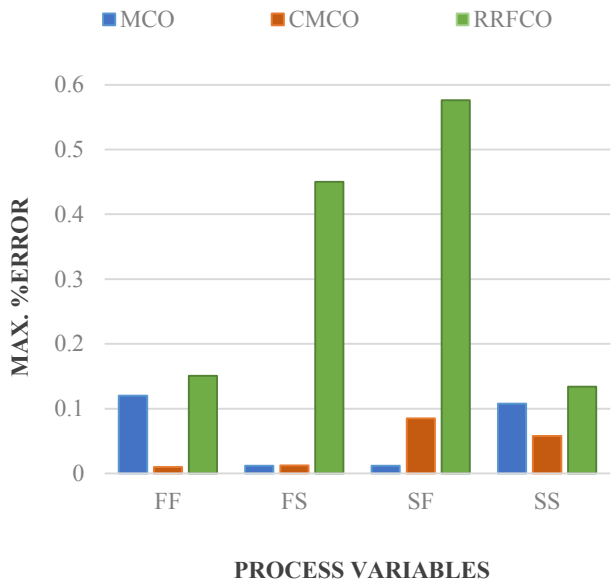

Fig.6. Maximum % error of the voltage obtained across the variable resistance Rsens for the three designed OTA topologies under process variations.

the two stage MCO and CMCO, a maximum percentage error always better than 0.12% is achieved.

V. CONCLUSION

The paper presented the design of three different OTA topologies used as voltage to current conversion circuit for gas sensing applications. High accuracy in converting the voltage signal is achieved when using the two stage OTAs that are the Miller Compensation and the Capacitor Multiplier Compensation OTAs. The performance of the designed OTAs was analyzed and compared. The corner simulations are also considered and presented to ensure the robustness of the design. Even not using a source follower output stage the designed OTAs managed to drive the large current load of 10mA and 1mA with a worst-case error of 0.02% under worst-case power supply and temperature conditions and a worst percentage error of 0.12% under process variation for both two stage MCO and CMCO.

REFERENCES

[1] A. j. Lopez-Martin, J. Ramirez-Angulo and R. G. Carvajal, "±1.5V 3mW CMOS V-to-I converter with 75 dB SFDR for 6V/sub pp/ input swings," in Electronics Letters, vol. 43, no. 6, pp. 31-32, March 15 2007.

[2] M. Grassi, P. Malcovati, and A. Baschirotto, "A 141-dB dynamic range CMOS gas-sensor interface circuit without calibration with 16- bit digital output word," IEEE J. Solid-State Circuits, vol. 42, no. 7, pp. 1543–1554, Jul. 2007.

[3] C. Azcona, B. Calvo, S. Celma, N. Medrano and P. A. Martínez, "Ratiometric Voltage-to-Frequency Converter for Long-Life Autonomous Portable Equipment," in IEEE Sensors Journal, vol. 13, no. 6, pp. 2382-2390, June 2013.

[4] F. Conso, M. Grassi, P. Malcovati, A. Baschirotto. "Reconfigurable Integrated Wide-Dynamic-Range Read-Out Circuit for MOX Gas- Sensor Grids Providing Local Temperature Regulation", proceedings of SENSORS'12, Taipei, Oct. 2012, pp.1822-1825, IEEE

[5] A. De Marcellis, G. Ferri, A. Depari and A. Flammini, "A novel time-controlled interface circuit for resistive sensors," Sensors, 2011 IEEE, Limerick, 2011, pp. 1137-1140.

[6] Willy M. C. Sansen, "Analog Design Essentials", Springer-Verlag New York, Inc. Secaucus, NJ, USA © 2006.

[7] Z. Yan, L. Shen, Y. Zhao and S. Yue, "Capacitor-Multiplier Frequency Compensation for Low-Power Multistage Amplifiers," Electronics, Circuits and Systems, 2007. ICECS 2007. 14th IEEE International Conference on, Marrakech, 2007, pp. 502-505.