A State-Space Approach to the Modelling and Control of the Neutral Leg of a Four Legs, Three-Phase Inverter

Massimiliano Passalacqua, *Member*, Gislain Grosjean, Simon Kissling, Mokhtar Bozorg, *Member,* Mario Marchesoni, *Member*, Mauro Carpita, *Member*

***Abstract*— In this paper, a novel approach to determine the model of an ICNL (Independently Controlled Neutral Leg) is proposed. Based on this model, a cascaded control method is developed to provide a steady neutral point connection for a three-phase four-wire inverter and to balance the two DC capacitors voltages of a split DC-bus. Validation of the model is realised by simulations and the control has been tested by experiments. Results have shown good performance even with a high level of neutral current, which demonstrate the ability of the system to work within an unbalanced load or grid.**

***Index Terms*— Neutral leg control, split DC-bus, three-phase four-wire inverter.**

I. INTRODUCTION

THE spreading of renewables and distributed generation in last decades has led to increase the use of grid-connected inverters. Indeed, inverters must be used to interface DC sources [1] (e.g. photovoltaics [2, 3] and storage systems) with the AC grid. Moreover, inverters could also be used to interface AC sources (e.g., wind-turbines [4, 5] or hydro-turbines) to the AC grid. AC source voltage and frequency may differ from the grid values, and they can vary according to the working point. In order to connect AC sources to the grid, two stages are generally used: a first inverter is used as a rectifier and the second inverter connects the so-obtained DC bus to the AC grid. In addition, inverters are also used for active power filter [6, 7] and uninterruptible power supply applications [8, 9]. Low voltage grids are usually 4-wire (i.e., three-phase with neutral connection), therefore an appropriate management of the neutral line should be conceived for the inverter. Various topologies and strategies have been proposed for this scope. Considering transformer-less structures, the simplest solution is to connect the neutral wire directly to the DC-link central point, obtaining a split DC-link topology [10-14]. Even though various balancing technique have been proposed [11, 14], the split DC-link topology is convenient when the neutral current does not have a DC component and the fundamental component is quite low, as in active filters [13]. If the neutral current is high and, especially, if it has a DC component, a fourth leg is needed to manage the neutral connection (conventional neutral leg topology) [15-18]. However, in this configuration, the neutral leg cannot be independently controlled, and therefore the overall system control strategy becomes rather complicated [19]. Another topology proposed in the literature [19, 20] is the independently controlled neutral leg, shown in Fig. 1. This is actually a combination of the two previous solutions.

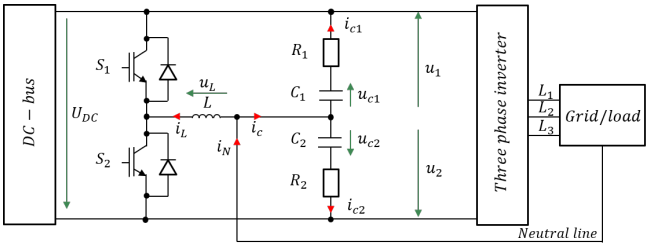


Fig. 1. Independently controlled neutral leg topology.

An analytical modelling of the independently controlled neutral leg (ICNL) was firstly proposed by Zhong et al. in [19], and an appropriate controller was defined and tuned. The main purpose of the neutral leg control is to minimize the DC-link voltage unbalance (i.e., the difference between the voltages of C_1 and C_2 in Fig. 1). However, the model proposed in [19] is somehow simplified, since it does not consider the capacitor parasitic resistances (i.e., R_1 and R_2 in Fig. 1), which have a

Manuscript received Month xx, 2xxx; revised Month xx, xxxx; accepted Month x, xxxx.

This work was partly supported by Romande Energie (CH) for the funding of the research presented in this paper in the frame of the REEL project. This research is part of the activities of the Swiss Centre for Competence in Energy Research on the Future Swiss Electrical Infrastructure (SCCER-FURIES), which is financially supported by the Swiss Innovation Agency (Innosuisse-SCCER program).

Gislain Grosjean, Simon Kissling, Mokhtar Bozorg and Mauro Carpita are with the University of Applied Sciences and Arts of Western Switzerland (HES SO), route de Cheseaux 1, 1401 Yverdon-les-Bains; e-mail: gislain.grosjean@heig-vd.ch, simon.kissling@heig-vd.ch, mokhtar.bozorg@heig-vd.ch and mauro.carpita@heig-vd.ch (corresponding author)).

Massimiliano Passalacqua and Mario Marchesoni are with the Department of Naval, Electrical, Electronic and Telecommunication Engineering, University of Genova, Genova 16145, Italy; e-mail: massimiliano.passalacqua@edu.unige.it, marchesoni@unige.it.

damping effect on the voltage unbalance. More important, it does not take into account the effect of the neutral current on the DC link terminals, because the neutral current is modelled as a perturbation coming from the neutral line. In this paper, a novel approach to determine the ICNL analytical model, which considers also capacitor parasitic resistances and the influence on the DC-link terminals of the neutral current, is carried out. The validity of the proposed model is verified by comparing the model output with the output of an accurate simulation model in MATLAB/Simulink PLECS environment, which simulates the behaviour of the overall system (i.e., neutral leg plus inverter). Once the transfer function between the neutral leg current and the fourth-leg duty cycle is determined and validated, a cascaded control of the capacitor's voltage unbalance is designed and tuned. The influence of a feed-forward action on the neutral current, and the compensation of the fourth-leg dead-time has been presented too. The controller performances are evaluated with both simulations and experimental results.

To summarize, the novelties of this paper are the introduction of the State Space model of the neutral control and the definition of a cascaded schematic for controlling the ICNL topology; in addition to that, the cascaded control is furtherly enhanced with the introduction of a feed-forward action and of a dead-time compensation.

The paper is structured as follows. The state-space ICNL analytical model is obtained in Section II. The PLECS model of the system and the validation of the obtained transfer function are shown in Section III. The neutral leg controller is designed in Section IV, simulated in Section V and experimentally validated in Section VI. Finally, conclusions are pointed out in Section VII.

II. INDEPENDENTLY CONTROLLED NEUTRAL LEG STATE-SPACE MODEL

A. Theoretical model

The model is based on the classical state approach as proposed by Middlebrook and Cuk [21]. To maintain the development as simple as possible, the fourth leg is supposed to work always in continuous conduction, even though an exact state-space model could be obtained in discontinuous mode too [22]. The considered neutral leg model is shown in Fig. 2. Let us consider a fully symmetrical system, i.e. the value of C_1 equal to C_2 (1), R_1 equal to R_2 (2) and that in steady-state the voltages on both the capacitors are equals.

$$C_1 = C_2 = C \tag{1}$$

$$R_1 = R_2 = R \tag{2}$$

We assume that the neutral current will split into two contributions at the positive and negative poles of the DC-link. With the full symmetry hypothesis, and the steady-state equilibria of the DC-link, we suppose that the two contributions are identical. i.e. the splitting factor is 50%. We will consider also that the current does not became zero during the switching period, i.e. as already said the discontinuous mode behaviour is not taken into account.

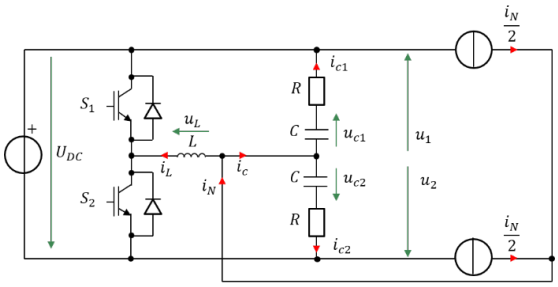


Fig. 2. Neutral leg model.

B. UP configuration

The UP configuration, when the upper switch S_1 is close, is shown in Fig. 3. The system of equations (3) can then be obtained.

$$\begin{cases} i_{DC} = -i_L - i_{c1} + \frac{i_N}{2} \\ i_N = i_L + i_{c1} + i_{c2} \\ U_{DC} = u_{c2} + Ri_{c2} - u_{c1} - Ri_{c1} \\ u_L = u_{c1} + Ri_{c1} \end{cases} \tag{3}$$

Substituting the inductor and capacitors state equations in (3) and resolving the system of equations for the state variables (i.e. i_L, u_{c1} and u_{c2}) one obtains equation's system (4), together with the equation (5) for the DC link current i_{DC}.

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{du_{c1}}{dt} \\ \frac{du_{c2}}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R}{2L} & \frac{1}{2L} & \frac{1}{2L} \\ -\frac{1}{2C} & -\frac{1}{2CR} & \frac{1}{2CR} \\ -\frac{1}{2C} & \frac{1}{2CR} & -\frac{1}{2CR} \end{bmatrix} \begin{pmatrix} i_L \\ u_{c1} \\ u_{c2} \end{pmatrix} + \begin{bmatrix} -\frac{1}{2L} & \frac{R}{2L} \\ -\frac{1}{2CR} & \frac{1}{2C} \\ \frac{1}{2CR} & \frac{1}{2C} \end{bmatrix} \begin{pmatrix} U_{DC} \\ i_N \end{pmatrix} \tag{4}$$

$$i_{DC} = \begin{bmatrix} -\frac{1}{2} & \frac{1}{2R} & -\frac{1}{2R} \end{bmatrix} \begin{pmatrix} i_L \\ u_{c1} \\ u_{c2} \end{pmatrix} + \begin{bmatrix} \frac{1}{2R} & 0 \end{bmatrix} \begin{pmatrix} U_{DC} \\ i_N \end{pmatrix} \tag{5}$$

Therefore, the system can be written in the form of equations (6) and the matrixes (7) and (8) can be defined.

$$\begin{cases} \frac{dx}{dt} = A_u\, x + B_u\, u \\ y = C_u\, x + E_u\, u \end{cases} \Rightarrow x = \begin{pmatrix} i_L \\ u_{c1} \\ u_{c2} \end{pmatrix};\ u = \begin{pmatrix} U_{DC} \\ i_N \end{pmatrix};\ y = i_{DC} \tag{6}$$

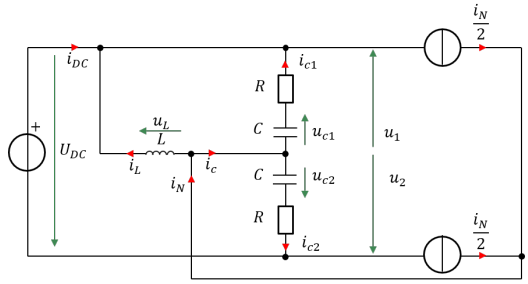


Fig. 3. Neutral leg circuit in configuration UP.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2021.3070495, IEEE Transactions on Industrial Electronics

$$A_u = \begin{bmatrix} -\frac{R}{2L} & \frac{1}{2L} & \frac{1}{2L} \\ -\frac{1}{2C} & -\frac{1}{2CR} & \frac{1}{2CR} \\ -\frac{1}{2C} & \frac{1}{2CR} & -\frac{1}{2CR} \end{bmatrix};\ B_u = \begin{bmatrix} -\frac{1}{2L} & \frac{R}{2L} \\ -\frac{1}{2CR} & \frac{1}{2C} \\ \frac{1}{2CR} & \frac{1}{2C} \end{bmatrix} \tag{7}$$

$$C_u = \begin{bmatrix} -\frac{1}{2} & \frac{1}{2R} & -\frac{1}{2R} \end{bmatrix};\ E_u = \begin{bmatrix} \frac{1}{2R} & 0 \end{bmatrix} \tag{8}$$

C. DOWN configuration

For the circuit in configuration DOWN, when the lower switch S_2 is closed as shown in Fig. 4, the system of equations (9) can be obtained.

$$\begin{cases} i_{DC} = i_L + i_{c2} - \frac{i_N}{2} \\ i_N = i_L + i_{c1} + i_{c2} \\ U_{DC} = u_{c2} + Ri_{c2} - u_{c1} - Ri_{c1} \\ u_L = u_{c2} + Ri_{c2} \end{cases} \tag{9}$$

By the same way than equations (4) and (5) above, one obtains equations (10) and (11) for the DOWN configuration.

Therefore, the system can be written in the form of equations (12) and the matrixes (13) and (14) can be defined.

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{du_{c1}}{dt} \\ \frac{du_{c2}}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R}{2L} & \frac{1}{2L} & \frac{1}{2L} \\ -\frac{1}{2C} & -\frac{1}{2CR} & \frac{1}{2CR} \\ -\frac{1}{2C} & \frac{1}{2CR} & -\frac{1}{2CR} \end{bmatrix} \begin{pmatrix} i_L \\ u_{c1} \\ u_{c2} \end{pmatrix} + \begin{bmatrix} \frac{1}{2L} & \frac{R}{2L} \\ -\frac{1}{2CR} & \frac{1}{2C} \\ \frac{1}{2CR} & \frac{1}{2C} \end{bmatrix} \begin{pmatrix} U_{DC} \\ i_N \end{pmatrix} \tag{10}$$

$$i_{DC} = \begin{bmatrix} \frac{1}{2} & \frac{1}{2R} & -\frac{1}{2R} \end{bmatrix} \begin{pmatrix} i_L \\ u_{c1} \\ u_{c2} \end{pmatrix} + \begin{bmatrix} \frac{1}{2R} & 0 \end{bmatrix} \begin{pmatrix} U_{DC} \\ i_N \end{pmatrix} \tag{11}$$

$$\begin{cases} \frac{dx}{dt} = A_d\, x + B_d\, u \\ y = C_d\, x + E_d\, u \end{cases} \Rightarrow x = \begin{pmatrix} i_L \\ u_{c1} \\ u_{c2} \end{pmatrix};\ u = \begin{pmatrix} U_{DC} \\ i_N \end{pmatrix};\ y = i_{DC} \tag{12}$$

$$A_d = \begin{bmatrix} -\frac{R}{2L} & \frac{1}{2L} & \frac{1}{2L} \\ -\frac{1}{2C} & -\frac{1}{2CR} & \frac{1}{2CR} \\ -\frac{1}{2C} & \frac{1}{2CR} & -\frac{1}{2CR} \end{bmatrix};\ B_d = \begin{bmatrix} \frac{1}{2L} & \frac{R}{2L} \\ -\frac{1}{2CR} & \frac{1}{2C} \\ \frac{1}{2CR} & \frac{1}{2C} \end{bmatrix} \tag{13}$$

$$C_d = \begin{bmatrix} \frac{1}{2} & \frac{1}{2R} & -\frac{1}{2R} \end{bmatrix};\ E_d = \begin{bmatrix} \frac{1}{2R} & 0 \end{bmatrix} \tag{14}$$

D. Average switching model

Exploiting the average switching model theory [21] one can define the matrixes in system of equations (15).

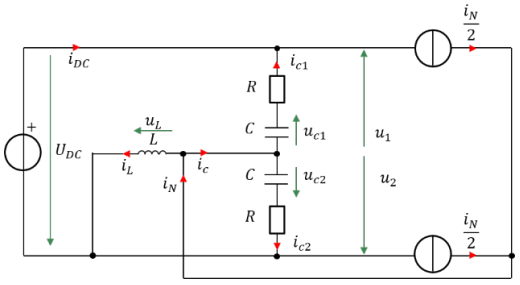


Fig. 4. Neutral leg circuit in configuration DOWN.

$$\begin{cases} A \coloneqq A_u d + A_d(1-d) \\ B \coloneqq B_u d + B_d(1-d) \\ C \coloneqq C_u d + C_d(1-d) \\ E \coloneqq E_u d + E_d(1-d) \end{cases} \tag{15}$$

Being d the duty cycle of the fourth (neutral) leg, $d = 1$ means the leg is in UP configuration, whereas $d = 0$ means the leg is in DOWN configuration. The system can then be written in the form of equations (16) and the matrixes (17) and (18) can be defined.

$$\begin{cases} \frac{dx}{dt} = A\, x + B\, u \\ y = C\, x + E\, u \end{cases} \Rightarrow x = \begin{pmatrix} i_L \\ u_{c1} \\ u_{c2} \end{pmatrix};\ u = \begin{pmatrix} U_{DC} \\ i_N \end{pmatrix};\ y = i_{DC} \tag{16}$$

$$A = \begin{bmatrix} -\frac{R}{2L} & \frac{1}{2L} & \frac{1}{2L} \\ -\frac{1}{2C} & -\frac{1}{2CR} & \frac{1}{2CR} \\ -\frac{1}{2C} & \frac{1}{2CR} & -\frac{1}{2CR} \end{bmatrix};\ B = \begin{bmatrix} \frac{1-2d}{2L} & \frac{R}{2L} \\ -\frac{1}{2CR} & \frac{1}{2C} \\ \frac{1}{2CR} & \frac{1}{2C} \end{bmatrix} \tag{17}$$

$$C = \begin{bmatrix} \frac{1}{2} - d & \frac{1}{2R} & -\frac{1}{2R} \end{bmatrix};\ E = \begin{bmatrix} \frac{1}{2R} & 0 \end{bmatrix} \tag{18}$$

One can define three functions (f_1, f_2 and f_3) which correspond to the state variable time derivative. These three functions are defined in equations (19), (20) and (21).

$$f_1 = \frac{di_L}{dt} = -\frac{R}{2L}\, i_L + \frac{1}{2L}\, u_{c1} + \frac{1}{2L}\, u_{c2} + \frac{1-2d}{2L}\, U_{DC} + \frac{R}{2L}\, i_N \tag{19}$$

$$f_2 = \frac{du_{c1}}{dt} = -\frac{1}{2C}\, i_L - \frac{1}{2CR}\, u_{c1} + \frac{1}{2CR}\, u_{c2} - \frac{1}{2CR}\, U_{DC} + \frac{1}{2C}\, i_N \tag{20}$$

$$f_3 = \frac{du_{c2}}{dt} = -\frac{1}{2C}\, i_L + \frac{1}{2CR}\, u_{c1} - \frac{1}{2CR}\, u_{c2} + \frac{1}{2CR}\, U_{DC} + \frac{1}{2C}\, i_N \tag{21}$$

Since (16) is a non-linear system (d is an input variable), a linearization process is required. Considering small variations δ of all the variables, the system (16) can be linearized as in equation (22) and the matrixes (23) and (24) can be defined.

$$\frac{d}{dt}\begin{pmatrix} \delta i_L \\ \delta u_{c1} \\ \delta u_{c2} \end{pmatrix} = \tilde{A}\begin{pmatrix} \delta i_L \\ \delta u_{c1} \\ \delta u_{c2} \end{pmatrix} + \tilde{B}\begin{pmatrix} \delta U_{dc} \\ \delta i_n \\ \delta d \end{pmatrix} \tag{22}$$

$$\tilde{A} = \begin{bmatrix} \frac{d}{di_L} f_1 & \frac{d}{du_{c1}} f_1 & \frac{d}{du_{c2}} f_1 \\ \frac{d}{di_L} f_2 & \frac{d}{du_{c1}} f_2 & \frac{d}{du_{c2}} f_2 \\ \frac{d}{di_L} f_3 & \frac{d}{du_{c1}} f_3 & \frac{d}{du_{c2}} f_3 \end{bmatrix} \tag{23}$$

$$\tilde{B} = \begin{bmatrix} \frac{d}{dU_{dc}} f_1 & \frac{d}{di_n} f_1 & \frac{d}{dd} f_1 \\ \frac{d}{dU_{dc}} f_2 & \frac{d}{di_n} f_2 & \frac{d}{dd} f_2 \\ \frac{d}{dU_{dc}} f_3 & \frac{d}{di_n} f_3 & \frac{d}{dd} f_3 \end{bmatrix} \tag{24}$$

Within the linearization process, nine different transfer functions can be evaluated. In order to define the system model, the transfer functions that correlate i_L to d (25) and to i_N (26) must be evaluated.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2021.3070495, IEEE Transactions on Industrial Electronics

$$\frac{\delta i_L}{\delta d} = \left[(sI - \tilde{A})^{-1}\tilde{B}\right]_{1,3} = -\frac{2CU_{dc}s}{2LCs^2+CRs+1} \quad (25)$$

$$\frac{\delta i_L}{\delta i_N} = \left[(sI - \tilde{A})^{-1}\tilde{B}\right]_{1,2} = -\frac{CRs+1}{2LCs^2+CRs+1} \quad (26)$$

By defining the DC-link voltage unbalance ε as in equation (27) and the DC link incoming current i_C as in equation (28), it is possible to obtain the transfer function correlating ε to i_C, which is shown in equation (29).

$$\varepsilon = U_{c1} + Ri_{c1} + U_{c2} + Ri_{c2} \quad (27)$$

$$i_c = i_{c1} + i_{c2} \quad (28)$$

$$\frac{\delta \varepsilon}{\delta i_c} = \frac{CRs+1}{Cs} \quad (29)$$

With equations (25), (26), (29) and by applying Kirchhoff's laws it is possible to represent the small variations block diagram of the system, as shown in Fig. 5.

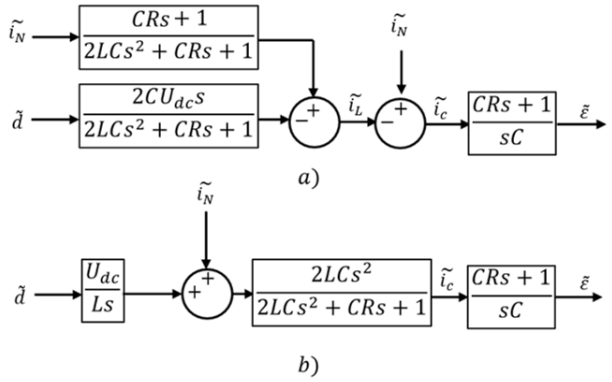


Fig. 5. Neutral leg transfer function of the system before (a) and after (b) being simplified.

III. MODEL VALIDATION

In order to validate the theoretical model and the obtained transfer functions, the three following models have been implemented in PLECS environment:

- the complete circuit with inverter (Fig. 1),
- the theoretical non-linear model (Fig. 2),
- the linearized small variation block diagram model (Fig. 5b).

The complete circuit with inverter means the actual simulation of the full system in the time domain.

The simulations parameters are reported in Table I.

TABLE I. SIMULATIONS PARAMETERS

Parameter	Value	Parameter	Value
R	750 µΩ	U_{dc}	800 V
L	1.5 mH	U_{ac}	400 V /50 Hz
C	100 µF	Switching frequency	15 kHz

All the three simulated systems are subjected to the same variations of the input variables. More precisely, the simulations have been performed considering small variations of the duty cycle and of the neutral current, as reported in Table II.

TABLE II. VARIATIONS DURING THE SIMULATION

Time	Duty cycle	Neutral current
0-30 ms	0.5	0 A
30-60 ms	0.5	2 A
60-100 ms	0.505	2 A

The validation is carried out by comparing the voltage unbalance (i.e., the difference between the actual capacitor voltages u_1 and u_2) of the three different systems. In Fig. 6 the response obtained with the complete model is shown (upper graphics), together with the difference between the theoretical non-linear model and the complete model (middle graphics) and eventually the difference between the small variation linearized block diagram model and the complete model (lower graphics). One can note that the differences in the last two behaviours are negligible compared to the complete model voltage unbalance and, therefore, the validation of the model is achieved. This allows the model to be confidently used for the control synthesis, as it will be shown in the next sections.

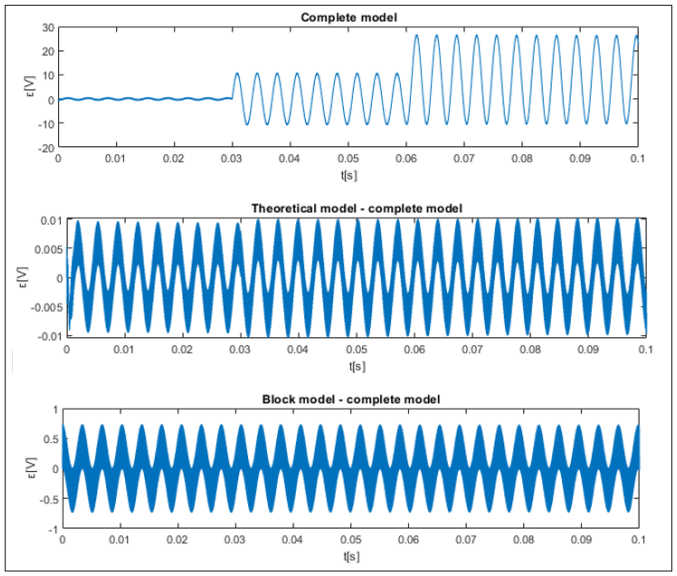


Fig. 6. Comparison of the voltage unbalance behaviour for the three different simulated systems. Upper graphics : Complete model behaviour. Middle graphics: Difference between the theoretical non-linear model and the complete model. Lower graphics: difference between the small variation linearized block diagram model and the complete model.

IV. NEUTRAL LEG CONTROL

A. Basic control

The neutral leg model proposed in Fig. 5b is used in this paper to design the control for the DC-link unbalance.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2021.3070495, IEEE Transactions on Industrial Electronics

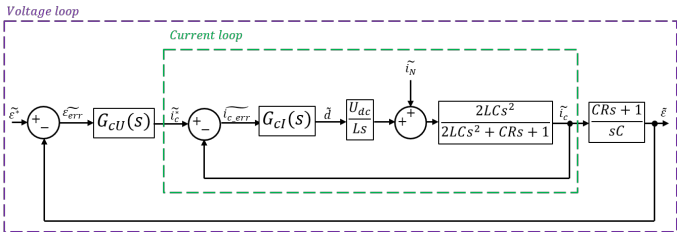


Fig. 7. Neutral leg control.

The proposed control has an inner current loop and an outer voltage loop, as shown in Fig. 7.

B. Inner current loop design

The current loop aims at minimizing the current incoming into the neutral connection of the two capacitors, despite the neutral current perturbation. Due to the integral behaviour of the system, a proportional gain is enough for this inner loop control. Using the Bode diagram of the system and taking into account the harmonics up to 30, the cut-off frequency (f_{c1}) value might be selected at 1.5 kHz. This is 10 time lower than the switching frequency, which is 15 kHz. The gain K_{pi} is defined in order to have -3 dB at the cut-off frequency, as shown in Fig. 8.

Another design issue is avoiding the LC resonance, shown in equation (30), be too close to the cut-off frequency. Equation (30) can be obtained from the block diagram in Fig. 5b, imposing $2LCs^2+CRs+1=0$ and neglecting the capacitor parasitic resistances. Indeed, the resistances have a damping effect but they have a low influence on the resonance frequency.

$$f_{res} = \frac{1}{2\cdot\pi\cdot\sqrt{2\cdot L\cdot C}} \tag{30}$$

This condition will help to careful choosing the value of the neutral inductance. The effect of the inner loop control on the neutral current perturbation is to reduce its impact at low frequency, as shown in Fig. 9.

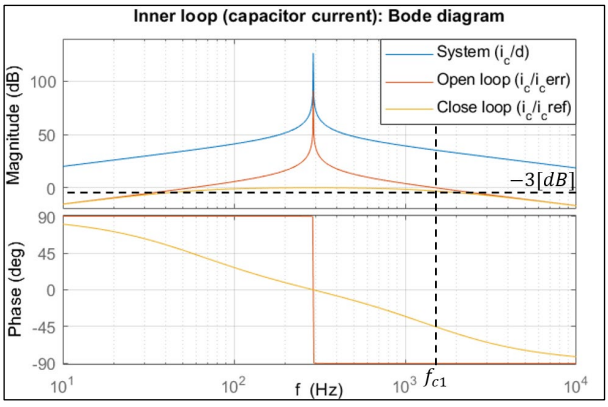


Fig. 8. Bode diagram of the inner loop system and its control (meaning of the variables in the legend).

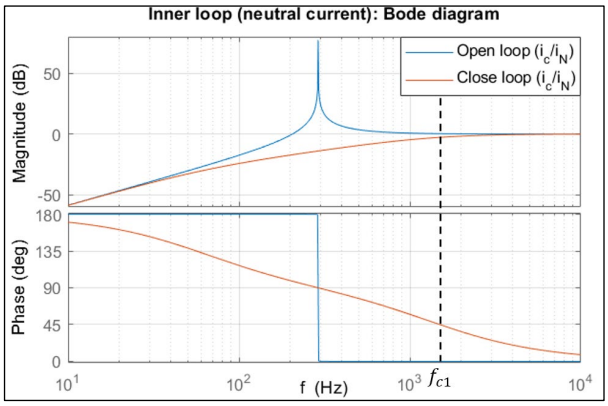


Fig. 9. Bode diagram of the inner loop related to the perturbation (meaning of the variables in the legend).

C. Outer voltage loop design

The voltage loop aims at keeping the DC-bus capacitor's voltage balanced. To guarantee a steady null value of the neutral point voltage, a proportional control again would be enough. However, by adding an integral part to the control, the reduction of the perturbation is more effective at low frequency. Using the Bode diagram of the outer loop system and choosing a phase margin of 60°, the gain K_{pu} can be defined as shown in Fig. 10. The integral gain can be obtained with the equation (31), where f_{c2} is the cut-off frequency of the outer loop, selected at 1.2 kHz.

$$K_{iu} = K_{pu}\frac{2\pi f_{c2}}{10} \tag{31}$$

The outer loop has a damping effect on the neutral current at high frequency as shown in Fig. 11. Moreover, as discussed above, a PI control is more effective to reduce the impact of the perturbation at low frequency.

D. Enhanced control

There are further approaches to improve the quality of the neutral leg control. Firstly, a feed-forward of the neutral current has been added, as shown in Fig. 12. This make the control more responsive to the impact of the neutral current on the voltage unbalancing.

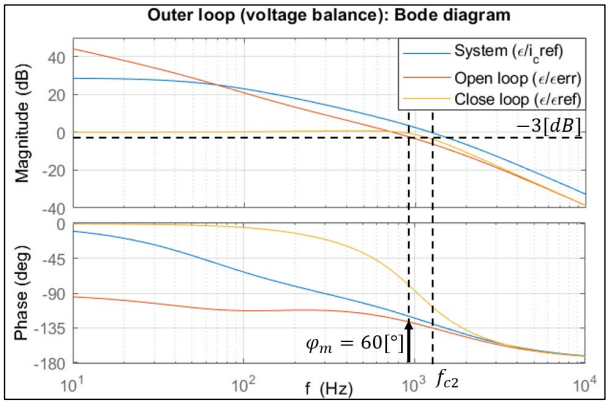


Fig. 10. Bode diagram of the outer loop system and its control (meaning of the variables in the legend).

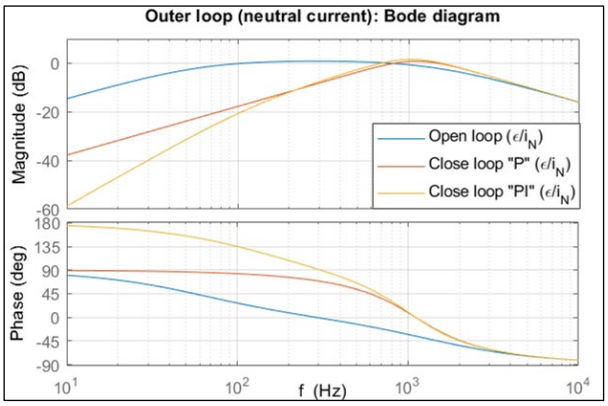


Fig. 11. Bode diagram of the outer loop related to the perturbation (meaning of the variables in the legend).

Secondly, a simple compensation of the fourth leg dead-time has been added. The required amount of voltage compensation ΔV can be evaluated as

$$\Delta V = \frac{U_{dc}}{2}\frac{t_{dead}}{T_{sw}} sign(i_n) \qquad (31)$$

where t_{dead} is the dead time, U_{dc} is the dc-link voltage, and T_{sw} is the inverter leg switching period [23]. Actually, this compensation should be based on a measurement of the inductor current. However, aim of the control is to make the neutral current approximatively equal to the inductor current. So, in order to reduce the number of measurements, it has been decided to use the neutral current instead of the inductor current. More sophisticated dead-time compensation strategies could have been implemented, but this is out of the main purposes of this paper.

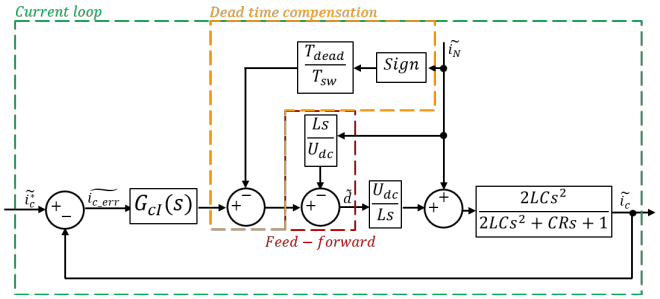


Fig. 12. Enhanced current control (p.u.).

V. Simulations

The control has been implemented in PLECS environment with the complete system (section III). Control parameters, as designed in section IV, are summarized in Table III.

The most usual neutral current perturbations are due to an unbalanced load/grid and to the harmonics generated by the modulation. For these reasons, the simulations have been done with a sinusoidal neutral current at the fundamental frequency and its three most important harmonics.

TABLE III. Control Parameters

Parameter	Value	Parameter	Value
K_{pu}	00.5 A/V	K_{iu}	378 A/V
K_{pi}	0.017 A^{-1}	T_{dead}	3 µs

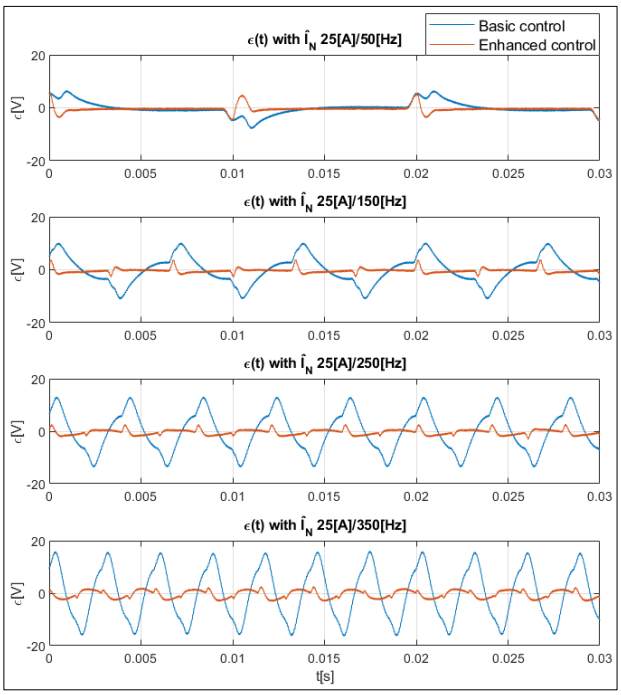


Fig. 13. Simulation results with a sinusoidal neutral current at different frequencies (fundamental, 3rd, 5th and 7th harmonics). The meaning of each graphic is described in the figure.

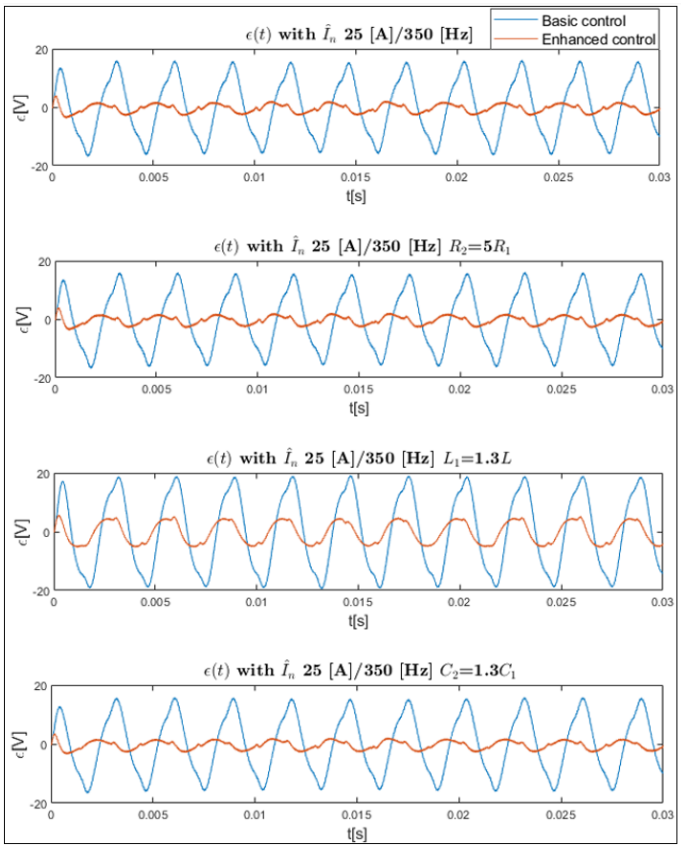


Fig. 14. Simulation results with a sinusoidal neutral current at 350 Hz and with different parameter uncertainties and unbalances. The meaning of each graphic is described in the figure.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2021.3070495, IEEE Transactions on Industrial Electronics

The simulation results are shown in as shown in Fig. 13. As it can be seen, the enhanced control has considerably improved the basic one results.

Simulation results in Fig. 13 were obtained considering $R=R_1=R_2$, $C=C_1=C_2$ and without uncertainty on the L value. In order to prove the robustness of the proposed control, additional simulations were carried out, by considering the following three cases:

- R_2 is five time R_1. This ratio has been chosen because capacitor parasitic resistances can vary significantly and they are not well known,
- L is 130% of the rated value (used in the controller synthesis),
- C_2 is about 30% higher than C_1.

As it can be noticed from Fig. 13, the case with 350 Hz neutral current is characterized by the highest oscillations amplitude, and then parameter uncertainty effects were evaluated for this frequency.

Simulation results are reported in Fig. 14. The robustness of the proposed controls is proven by the voltage unbalance being almost the same in all conditions.

VI. EXPERIMENTAL RESULTS

Experimental tests have been performed in order to validate the control concepts proposed in section IV. The neutral current has been generated by a single-phase half-bridge current controlled converter instead of a three-phase inverter, as shown in Fig. 15.

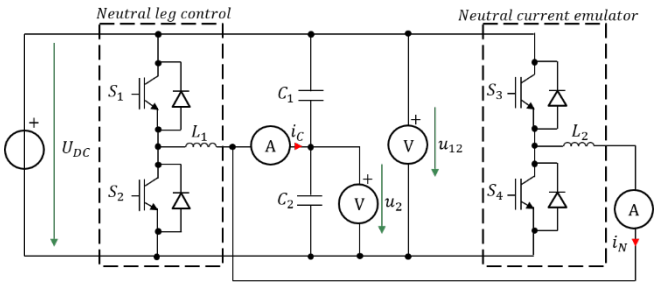


Fig. 15. Experimental circuit schematics.

Fig. 16. Experimental setup: Three-phase inverter, modified according to the schematic shown in Fig. 15; Two inductances only have been actually used.

TABLE IV. EXPERIMENTAL VALUES AND PARAMETERS

Parameter	Value	Parameter	Value
$L_1 = L_2$	1.5 mH	U_{dc}	800 V
$C_1 = C_2$	100 µF	f_{sw}	15 kHz
K_{pu}	0.5 A/V	K_{iu}	378 A/V
K_{pi}	0.017 AA^{-1}	T_{dead}	3 µs

The experimental setup is shown in Fig. 16. A previous existing three-phase inverter was modified in order to realize the circuit of Fig. 15. The experimental setup requires only two of the three inductors shown in Fig. 16. Experimental values and parameters are summarized in Table IV. The voltage values on C_1 and C_2 were measured with differential probes, the measures were exported from the oscilloscope and plotted using MATLAB; in this way it was possible to overlap results of different tests as plotted in Fig. 17.

The control has been tested up to the seventh neutral current harmonics, with an amplitude of 25 A for each harmonics. As shown in Fig. 17, the proposed control has shown a good ability to stabilise the neutral point, even with important values of the neutral current. The experimental values of the neutral voltage are analogous to the simulations' results.

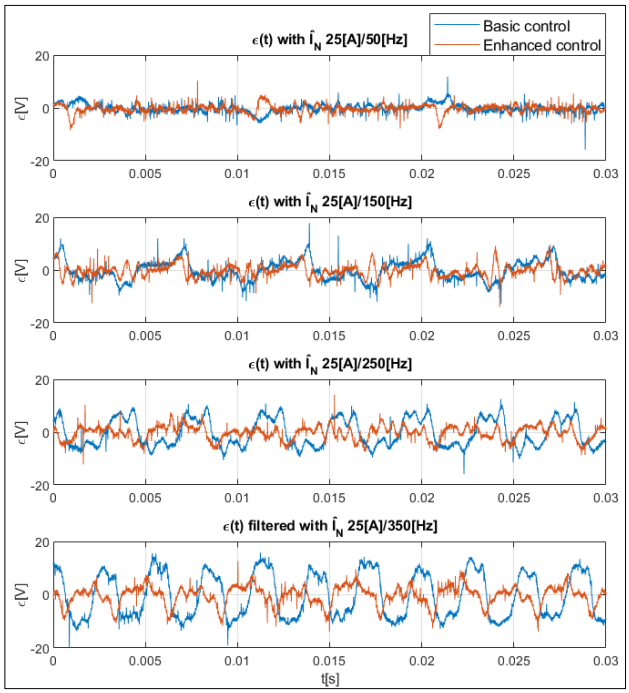


Fig. 17. Experimental results with a sinusoidal neutral current at different frequencies.

In order to quantify the effect of both the neutral voltage unbalance strategies, the RMS values of the voltage unbalance have been calculated and compared in Table V. The chosen capacity, 100 µF, has been purposely selected low enough to maximise the voltage unbalance and to appreciate the behaviour of the control system. The overall experimental results have shown the good ability of the enhanced control to improve the neutral point stability.

TABLE V. NEUTRAL VOLTAGE UNBALANCE COMPARISON

Neutral current	Ɛ basic control	Ɛ enhanced control	Difference
25 A peak @ 50 Hz	1.74 Vrms	1.70 Vrms	-2.3 %
25 A peak @ 150 Hz	3.86 Vrms	2.38 Vrms	-38 %
25 A peak @ 250 Hz	5.71 Vrms	2.75 Vrms	-52 %
25 A peak @ 350 Hz	8.46 Vrms	3.81 Vrms	-55 %

VII. CONCLUSION

A State Space approach to the modelling of an independently controlled neutral leg has been proposed and validated. This model has put in evidence the previously neglected resonance effect of the system. Based on this model, a cascaded control has been proposed, simulated and tested by experimental tests. The results have shown the validity of the proposed control to provide a steady neutral line for a four-wire three-phase inverter even with high neutral current. Furthermore, an enhanced control with feed-forward and dead time compensation has been implemented. The enhanced control has shown improved results both in simulations and in tests. By exploiting the proposed model, other forms of control can be studied, and this will be the subject of future investigations.

ACKNOWLEDGMENT

The authors gratefully acknowledge Serge Gavin, Guillaume Courteau and Mohammad Rayati for their contributions to the work presented in this paper.

REFERENCES

[1] X. Yan, Y. Cui and S. Cui, "Control method of parallel inverters with self-synchronizing characteristics in distributed microgrid," Energies 2019, vol. 12, no. 20, p. 3871.

[2] Y. Yoo, et al., "Accuracy improvement method of energy storage utilization with DC voltage estimation in large-scale photovoltaic power plants," Energies 2019, vol. 12, no. 20, p. 3907.

[3] A. Cabrera-Tobar, E. Bullich-Massagué, M. Aragüés-Peñalba and O. Gomis-Bellmunt, "Active and reactive power control of a PV generator for grid code compliance," Energies 2019, vol. 12, no. 20, p. 3872.

[4] Y. Ma, F. Zhao, X. Zhou, M. Liu and B. Yang, "DC side bus voltage control of wind power grid-connected inverter based on second-order linear active disturbance rejection control," Energies 2019, vol. 12, no. 22, p. 4274.

[5] X. Zhou, M. Liu, Y. Ma, B. Yang, and F. Zhao, "Linear active disturbance rejection control for DC Bus voltage of permanent magnet synchronous generator based on total disturbance differential," Energies 2019, vol. 12, no. 20, p. 3906.

[6] H. Li, S. Li, J. Lu, Y. Qu, and C. Guo, "A novel strategy based on linear active disturbance rejection control for harmonic detection and compensation in low voltage AC microgrid," Energies 2019, vol. 12, no. 20, p. 3982.

[7] C. I. Chen, C. K. Lan, Y. C. Chen, and C. H. Chen, "Adaptive frequency-based reference compensation current control strategy of shunt active power filter for unbalanced nonlinear loads," Energies 2019, vol. 12, no. 16, p. 3080.

[8] Y. Danayiyen, K. Lee, M. Choi, and Y. I. Lee, "Model predictive control of uninterruptible power supply with robust disturbance observer," Energies 2019, vol. 12, no. 15, p. 2871.

[9] Z. Rymarski, K. Bernacki, Ł. Dyga, and P. Davari, "Passivity-based control design methodology for UPS systems," Energies 2019, vol. 12, no. 22, p. 4301.

[10] Z. Lin, X. Ruan, L. Jia, W. Zhao, H. Liu and P. Rao, "Optimized design of the neutral inductor and filter inductors in three-phase four-wire inverter with split DC-link capacitors," in IEEE Transactions on Power Electronics, vol. 34, no. 1, pp. 247-262, Jan. 2019.

[11] R. Zhang, V. H. Prasad, D. Boroyevich and F. C. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converters," in IEEE Transactions on Power Electronics, vol. 17, no. 3, pp. 314-326, May 2002.

[12] P. Verdelho and G. D. Marques, "Four-wire current-regulated PWM voltage converter," in IEEE Transactions on Industrial Electronics, vol. 45, no. 5, pp. 761-770, Oct. 1998.

[13] C. A. Quinn and N. Mohan, "Active filtering of harmonic currents in three-phase, four-wire systems with three-phase and single-phase nonlinear loads," [Proceedings] APEC '92 Seventh Annual Applied Power Electronics Conference and Exposition, Boston, MA, USA, pp. 829-836, 1992.

[14] N. Dai, M. Wong, F. Ng and Y. Han, "A FPGA-based generalized pulse width modulator for three-leg center-split and four-leg voltage source inverters," in IEEE Transactions on Power Electronics, vol. 23, no. 3, pp. 1472-1484, May 2008.

[15] X. Guo, Y. Yang, R. He, B. Wang and F. Blaabjerg, "Transformerless Z-source four-leg PV inverter with leakage current reduction," in IEEE Transactions on Power Electronics, vol. 34, no. 5, pp. 4343-4352, May 2019.

[16] X. Guo, R. He, J. Jian, Z. Lu, X. Sun and J. M. Guerrero, "Leakage current elimination of four-leg inverter for transformerless three-phase PV systems," in IEEE Transactions on Power Electronics, vol. 31, no. 3, pp. 1841-1846, March 2016.

[17] A. L. Julian, G. Oriti and T. A. Lipo, "Elimination of common-mode voltage in three-phase sinusoidal power converters," in IEEE Transactions on Power Electronics, vol. 14, no. 5, pp. 982-989, Sept. 1999.

[18] T. M. Jahns, R. W. A. A. De Doncker, A. V. Radun, P. M. Szczesny and F. G. Turnbull, "System design considerations for a high-power aerospace resonant link converter," in IEEE Transactions on Power Electronics, vol. 8, no. 4, pp. 663-672, Oct. 1993.

[19] Q. C. Zhong, and T. Hornik, "Control of power inverters in renewable energy and smart grid integration, " John Wiley & Sons, vol. 97, 2012.

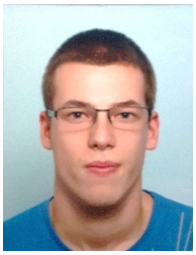
[20] Q. C. Zhong, L. Hobson, and M.G. Jayne, "Classical control of the neutral point in 4-wire 3-phase DC-AC converters," Electrical Power Quality and Utilisation, Journal, vol. 11, no. 2, pp. 73-81, 2005.

[21] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," 1976 IEEE Power Electronics Specialists Conference, Cleveland, OH, 1976, pp. 18-34.

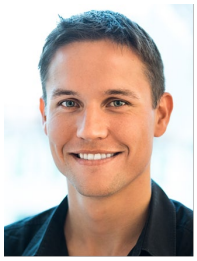
[22] M. Carpita, M. De Vivo and S. Gavin, "Dynamic modelling of a bidirectional DC/DC interleaved converter working in discontinuous mode for stationary and traction supercapacitor applications," International Symposium on Power Electronics Power Electronics, Electrical Drives, Automation and Motion, Sorrento, 2012, pp. 1306-1313.

[23] B. Chappuis, S. Gavin, L. Rigazzi and M. Carpita, "Speed Control of a Multiphase Active Way Linear Motor Based on Back EMF Estimation," in IEEE Transactions on Industrial Electronics, vol. 62, no. 12, pp. 7299-7308, Dec. 2015.

Massimiliano Passalacqua (S' 19) was born in Genoa, Italy in 1993. He received the B.S. (Hons.) degree and the M.S. (Hons) degree in electrical engineering from the University of Genoa in 2015 and 2017, respectively. He is currently a Ph.D. student at the Department of Electrical, Electronic and Telecommunication Engineering and Naval Architecture (DITEN) at the University of Genoa. His research interests include power electronics, control for electrical drives and hybrid electric vehicles.



Gislain Grosjean was born in Vucherens, Switzerland in 1995. He received the B.S. degree in electrical engineering from the University of Applied Sciences of Western Switzerland, Yverdon-les-Bains, Switzerland, in 2019. After graduation, he worked as a Researcher in the Institute of Energy and Electrical Systems, University of Applied Sciences of Western Switzerland, Yverdon-lesBains, Switzerland, in the power electronics field. His research interests include power electronics converter for high voltage applications, modular multilevel converters and STATCOM applications.



Simon Kissling was born in Yverdon-les-Bains, Switzerland, in 1986. He received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Applied Sciences Western Switzerland, Yverdon-les-Bains, Switzerland, in 2008 and 2012. He worked as Senior Electronics Engineer in DEPsys SA, Puidoux, Switzerland, in the field of high power welding supplies, motor control and power distribution grid monitoring. Since 2018, he is a Researcher with the Institute of Electrical Energy, University of Applied Sciences Western Switzerland, working in the power electronics field. His research interests include power electronics converters for high-voltage applications, multilevel converters, and high efficiency motor control.

Mokhtar Bozorg (M'11) received the M.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran (2008), and the Ph.D. degree from the École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland (2015). From 2015 to 2018, he was a Post-Doctoral Fellow and the Guest Scientist with Distributed Electrical System Laboratory, EPFL. Since 2019, he has been an Associate Professor in energy and power systems with the University of Applied Sciences Western Switzerland. His research interest includes smart grids, applications of mathematical modeling and optimization techniques in power systems, and integration of renewables and storage systems into power grids.

Mario Marchesoni (M'89) received the M.S. (Hons.) degree in electrical engineering and the Ph.D. degree in electrical engineering in power electronics from the University of Genova, Genova, Italy, in 1986 and 1990, respectively. Following his graduation, he began his research activity with the Department of Electrical Engineering, University of Genova, where he was an Assistant Professor from 1992 to 1995. From 1995 to 2000, he joined the Department of Electric and Electronic Engineering, University of Cagliari, Cagliari, Italy, where he was a Full Professor of power industrial electronics. Since 2000, he has been with the University of Genova, where he is currently a Full Professor of electrical drives control. His research interests include power electronics, with particular reference to high power systems for grid and motor applications, electrical systems for transportation, electrical drives, electrical machines, and automatic control. Dr. Marchesoni was the General Chairman of the EPE'19 ECCE Europe Conference. His technical and scientific activity, certified by about 200 papers mainly presented at international conferences and published on international journals, has been carried out within research contracts and cooperations with national and international companies.

Mauro Carpita (M'99) received the M.S. and Ph.D. degrees in electrical engineering from the University of Genoa, Genoa, Italy, in 1985 and in 1989, respectively. Following graduation, he was with the corporate research unit of Ansaldo, Genova, working in the field of converters for drives and power quality. From 1997 to 1999, he was a Technical Office Manager of power electronics welding machines with Lincoln Electric, Savona, Italy. From 1999 to 2003, he was a Senior Scientist working in the field of servo and very high speed drives with ABB Ricerca, Milan, Italy, and later with ABB Servomotors, Asti, Italy. Since 2003, he has been a Full Professor with the University of Applied Sciences and Arts of Western Switzerland, Yverdon-les-Bains, Switzerland. From 2013 he is the Head of the Institute of Energy and Electrical Systems of the same university. His research interests include power electronics and automatic control, particularly in High-Power Converters, High Voltage Converters and Smartgrids applications.. He is the author or co-author of about 100 papers mainly presented at international conferences and published on international journals. He is the holder of seven industrial patents. Dr. Carpita is a member of the European Power Electronics and Drives Association (EPE)