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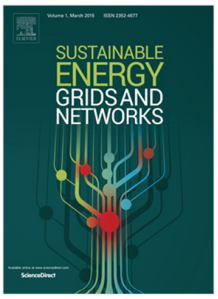

Design, realization and testing of a synthetic inertia controller for wind turbine power generators

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Design, Realization and Testing of a Synthetic Inertia Controller for Wind Turbine Power Generators

Andrea Bonfiglio[a,*], Matteo Lodi[a], Alessandro Rosini[a], Alberto Oliveri[a], Renato Procopio[a]

[a]*Department of Electrical, Electronic, Telecommunications Engineering and Naval Architecture, University of Genoa, Via Opera Pia 11a, Genova, 16145, Italy*

Abstract

The progressive inclusion of Renewable Energy Sources (RES) in power grids is causing a reduction of the overall system inertia, leading to a reduction of the system resiliency. A possible solution is equipping RES with synthetic inertia controllers so that additional power can be provided in case of severe frequency transients. This work reports the results of a research activity that aimed at improving the maturity of synthetic inertia controllers for wind turbine generators through the design and implementation of a controller prototype based on an advanced version of a synthetic inertia controller. Hardware-in-the-loop simulations are performed to validate the correct behavior of the prototype.

Keywords: Synthetic Inertia, Wind Turbine Generator, FPGA

1. Introduction

In recent years, climate changes, global warming, and the increasing price of fossil fuels have sped up the road-map for the decarbonization of the electricity system and the massive deployment of Renewable Energy Sources (RES) [1]. RES are a key part of the energy transition, nonetheless, the paradigm change from a synchronous-machine-based power system to a power-converter-dominated one brings in new challenges and problems that need to be faced in a timely and effective way. One of the issues caused

*Corresponding author
Email address: a.bonfiglio@unige.it (Andrea Bonfiglio)

by power generation connected to the grid through power converters is its incapability to contribute to inertial frequency support. This is leading to a reduction of the overall system inertia due to the dismissal (or temporary put out of production) of conventional power generators, in favor of RES [2]. A weakening of the electric inertia of the power grid can result in a destabilization of the system after major events, such as generation loss or a power system split, with a consequent risk of partial blackouts [3]. For this reason, several Transmission System Operators (TSOs) are introducing specific requirements for RES to make them more and more involved in frequency support [4]. The request for synthetic inertia is one of these upcoming requirements and a key element in providing an effective limitation of the Rate of Change of Frequency (RoCoF), an indicator that TSOs need to keep under control to guarantee the resiliency of the electricity system.

The study of synthetic inertia is not that new from an academic point of view. Some examples of the possibility of providing inertial support via a control action on power electronic devices are present in literature, from the initial application on wind turbine generators (WTGs) [5, 6] to more recent ones related to battery storage systems [7, 8] and photovoltaic power plants [9]. Despite a large amount of academic research on synthetic inertia technology, its maturity is not as advanced as other technologies under evaluation for the flexibilization of the electric power system [10]. For example, Virtual Power Plants (VPP), i.e., the aggregation of distributed renewable energy generation and batteries to enable the participation in balancing wholesale or flexibility markets, after a first phase of theoretical and academic investigation, have undergone a path of implementation and demonstration to prove the effectiveness and feasibility of the technology and its capability to reach a commercial application [11]. Currently, VPP are classified as Technology Readiness Level (TRL) 7, meaning that their functioning has been demonstrated in a real operational environment [12]. VPP are just an example of the importance of increasing the TRL of innovative power system technologies. Other examples can be found in microgrids management [13], DC grids protection [14], advanced control strategies, novel electricity conversion machines [15], and traditional power generators [16].

On the other hand, synthetic inertia technology is still characterized by a low TRL, but the fast migration of the power system is pushing TSOs to introduce inertial support services, that begin to be cited in some grid code requirements [17, 18]. From the academic point of view, researchers developed many strategies to provide inertial Frequency Support (FS): the

state of art solutions can be categorized into hidden inertia emulation [5] and fast power reserve [19]. The first category aims at mimicking the dynamic behavior of a synchronous generator, whereas the second one acts on the system providing active power for a specified amount of time.

An interesting innovative approach for providing FS, referred to as Variable Hidden Inertia Emulator (VHIE), has been presented in [20]. The VHIE controller provides an FS proportional to the RoCoF, avoiding instabilities due to excessive rotor speed reduction, and gives the maximum inertial contribution at the beginning of the frequency transient. Moreover, this solution includes a Rotor Speed Recovery (RSR) phase that minimizes the secondary frequency drop, compared to the state-of-the-art techniques, and the definition of a logic to manage the activation and deactivation of all the phases of the support action.

The practical implementation and realization of the VHIE controller (and synthetic inertia controllers, in general) might highlight technical issues relevant to the real application of the technology. In particular, the real inertia contribution of the controller may be affected by measurement noise and delays, circuit latency, distortions due to signal filtering, and quantization errors. This results in a late and altered response, corresponding to an inertia value different from the desired one. For this reason, the main focus of this article is to increase the technology maturity of the VHIE controller, thus reducing the gap for its final application in a real environment. This process is often not an easy task because, after the theoretical study, deployment and prototyping usually bring up problems and open issues that cannot be foreseen in the theoretical assessment.

This paper describes the implementation of the proposed logic in an embedded system, with specific reference to the problem of achieving a reliable evaluation of the RoCoF, the definition of the suitable interfacing signals for the communication between the prototype and the WTG controllers, the design of a dedicated interfacing board, and the influence of measurement noise on the system performance. The frequency measurements are performed through a high-performance off-the-shelf transducer, included as a part of the system. The final result is a laboratory prototype of the VHIE controller that has been tested in a Hardware In the Loop (HIL) fashion on a WTG model running on SpeedGoat *real-time* simulator. The validation has been carried on in several WTG operational scenarios and with different values of the controller inertia constant. The research results highlight that the response of the laboratory prototype is coherent with the software

simulation results, with an added delay and noise, as expected. This work paves the way for evaluating the impact of these real-world phenomena for both the compliance with TSO grid code requirements and the effectiveness of the inertial support provided by the WTG.

The hardware implementation of the VHIE controller allows taking into account: analog measurement noise, quantization errors introduced by analog-to-digital/digital-to-analog converters (ADCs/DACs), the latency of the FPGA and converters, delay and inaccuracy of e real frequency transducer, the effect of fixed point data representation. The paper results also represent an important step in the technological advancement of innovative synthetic inertia controllers, that are essential for the electricity system to withstand a sustainable transition to the massive integration of RES.

The paper is organized as follows: Section 2 describes the considered wind generator system and recalls the main features of the VHIE controller, whereas Section 3 focuses on the VHIE controller implementation of the controller hardware. The hardware prototype is described in Section 4, whereas the results of the HIL experimental validation are reported in Section 5. Finally, some conclusions are drawn in Section 6.

2. Wind Generator System

The functional scheme of a full-converter (Type4) WTG, with its main controllers, connected to a grid is shown in Fig. 1. This configuration accounts for a back-to-back converter and a Permanent Magnet Synchronous Generator (PMSG). The Machine Side Converter (MSC) rectifies the AC power provided by the generator, working at variable speed, whereas the DC-link and the Grid Side Converter (GSC), used as an inverter, allow the WTG connection to a fixed-frequency park distribution infrastructure. The GSC output voltage is raised through a low-voltage/medium-voltage (LV/MV) transformer, to be compatible with the wind farm distribution. Additional wind power plants with the same layout are connected to the wind park distribution infrastructure. The connection to the high-voltage transmission grid is realized through a medium-voltage/high-voltage (MV/HV) step-up transformer.

The MSC controller aims at regulating the wind generator's active power by following the Maximum Power Point Tracking (MPPT) algorithm reference. The maximum power point is usually defined as an algebraic function of the turbine rotor speed [21]. The GSC controller regulates the DC link

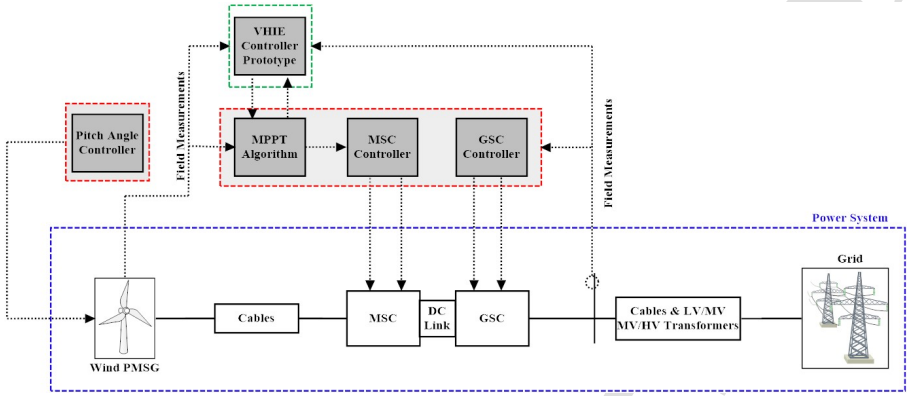


Figure 1: Functional scheme of a grid-connected WTG, with the conventional and VHIE controllers.

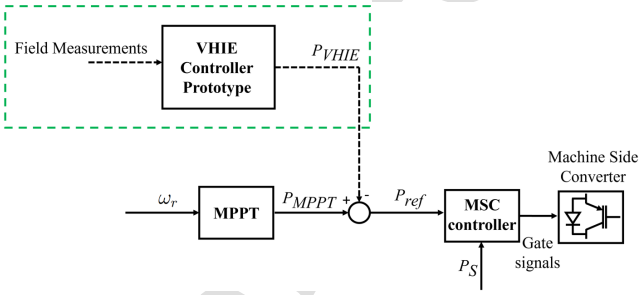


Figure 2: Integration of the VHIE controller prototype with the turbine control.

voltage and the reactive power to provide voltage support services to the grid if required. Finally, the pitch angle controller acts on the pitch angle of the wind turbine blades to limit the rotor speed to the maximum operational value, in case of strong wind. This action corresponds to a WTG output power limitation.

2.1. Variable Hidden Inertia Emulation Controller

As sketched in Fig. 2, the MSC controller receives in input a reference power

$$P_{ref} = P_{MPPT}(\omega_r) - P_{VHIE} \tag{1}$$

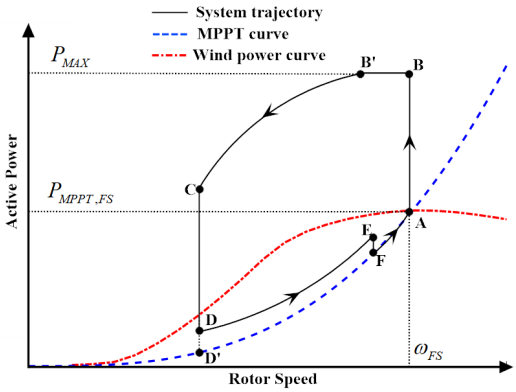


Figure 3: Qualitative effect of the VHIE controller on the wind turbine system.

where P_{MPPT} is the WTG MPPT reference and P_{VHIE} is an additional power (either positive or negative) provided by the VHIE controller. The MPPT reference depends on the turbine rotor speed ω_r [22], in particular:

$$P_{MPPT} = \begin{cases} 0, & \text{if } \omega_r < \omega_{r,cutin} \\ P_{max}\left(\frac{\omega_r}{\omega_{r,max}}\right)^3, & \text{if } \omega_{r,cutin} \leq \omega_r < \omega_{r,max} \\ P_{max}, & \text{if } \omega_r \geq \omega_{r,max} \end{cases} \tag{2}$$

being $\omega_{r,cutin}$ the cut-in rotor speed, $\omega_{r,max}$ the maximum rotor speed and P_{max} the maximum WTG power.

The VHIE controller operation [20] is divided into an FS phase, to provide synthetic inertia to the grid by avoiding undesired disconnection of the WTG, and an RSR phase, which regulates the rotor speed. The two phases are activated through a dedicated management logic. The main features of the VHIE controller, necessary for the understanding of the controller implementation and experimental validation are reported in the following. More information and details can be found by the interested reader in [20].

The evolution of an inertial frequency support transient is qualitatively reported in Fig. 3, where the red dashed curve represents the wind power at a given wind speed as a function of the rotor speed, with null pitch angle; the blue curve is the MPP profile [21], whereas the black curves denote the

overall power request (including the inertial contribution). If the black curve is above the red one, the requested power is greater than the power provided by the wind, which causes a rotor speed deceleration and vice-versa.

In normal operation the wind turbine is regulated to operate at its maximum power, i.e., at the intersection between the red and blue curves (point A). When grid frequency support is required, the VHIE controller enters the FS mode and provides additional power, thus moving the operating point to B. As the power production is greater than the wind power, the rotor speed decreases and the system evolves towards point C, where the FS mode ends according to FS disabling criteria [20]. The decrease of the power reference in FS is due to the reduction of both the MPPT reference signal and the additional (inertial) reference power, which is proportional to the rotor speed to prevent the WTG from undesired stalls. Segment B-B' in the black curve during FS indicates the possibility of a limitation of the deliverable power, due to the inverter's current rating. Once the FS phase is over (point C), the controller enters the RSR mode (point D) aimed at bringing the system back to point A. The position of point D is to be chosen as a compromise between a fast RSR and a limitation of the secondary frequency drop. If no RSR action is provided, the system moves to point D' on the MPPT curve, which implies a faster speed recovery with a larger secondary frequency drop. On the contrary, if a higher power is requested (point D closer to the red curve), the frequency drop is limited at the cost of a longer speed recovery time. The VHIE controller chooses the position of point D through a measurement of the system frequency, to evaluate whether a larger secondary frequency drop is affordable. Once the system is sufficiently close to the MPPT curve (point E) the RSR phase terminates and the VHIE controller becomes inactive (point F on the MPPT curve) so that the system naturally evolves back to point A.

The controller inputs (all in p.u.) are the electrical frequency f_e at the GSC output, the wind turbine rotor speed ω_r, the reference power P_{ref}, the maximum power point tracking power P_{MPPT} and the wind power P_{wind}. f_e can be measured through a frequency transducer, as will be detailed in the following, ω_r can be measured through a speed sensor in the turbine rotor (already used in the wind power controller for the MPPT power calculation), P_{MPPT} and P_{ref} are available control signals and P_{wind} can be calculated on

the basis of wind speed measurement, as

$$P_{wind} = \frac{\rho A_r C_p(\lambda, \beta) v_w^3}{2P_n} \tag{3}$$

being ρ the air density (in kg/m^3), A_r the rotor area (in m^2), v_w the wind speed (in m/s), and P_n the nominal power (in W). The aerodynamic coefficient C_p (dimensionless) depends on the pitch angle β (in degrees) and on the tip speed ratio $\lambda = \frac{R\omega_r\omega_{r,n}}{v_w}$, where $\omega_{r,n}$ is the nominal rotor speed (in rad/s) and R is the radius of the turbine [22]. If the wind speed measurement is not available, P_{wind} can be estimated based on other quantities within the WTG control and monitoring system [21]. The controller's output is the additional reference power P_{VHIE}.

When the grid is at steady state (point A in Fig. 3), the VHIE controller is inactive. The FS mode is activated when the RoCoF decreases below a given negative threshold, namely $RoCoF_{act}$:

$$\frac{df_e}{dt} \leq RoCoF_{act} \tag{4}$$

The rotor speed and the MPPT power at the beginning of the FS operation are denoted as $\omega_{r,FS}$ and $P_{MPPT,FS}$, respectively.

The controller switches to the RSR mode when either (i) the RoCoF exceeds a threshold $RoCoF_{deact}$, (ii) the reference power P_{ref} goes below the MPPT power $P_{MPPT,FS}$ at the beginning of the FS, or (iii) the FS time t_{FS} exceeds a threshold T_{FS}:

$$\frac{df_e}{dt} \geq RoCoF_{deact} \text{ U } P_{ref} \leq P_{MPPT,FS} \text{ U } t_{FS} > T_{FS} \tag{5}$$

The electrical frequency at the beginning of the RSR operation is denoted as $f_{e,RSR}$.

The RSR operation ends when the difference between the reference and the MPPT power is lower than a given threshold ΔP_s:

$$P_{ref} - P_{MPPT} \leq \Delta P_s \tag{6}$$

Then, the VHIE controller goes back to the inactive state. Notice that conditions (5) and (6) can be both satisfied, e.g., when the rotor speed (and then P_{MPPT}) does not decrease too much in the FS phase, then the RSR operation can be possibly skipped.

The output additional reference power P_{VHIE} is defined as:

$$P_{VHIE} = \begin{cases} 0, \quad \text{(inactive)} & (7) \\ 2H \dfrac{\omega_r - \omega_{r,min}}{\omega_{r,FS} - \omega_{r,min}} f_e \dfrac{df_e}{dt}, \quad \text{(FS)} & (8) \\ K_{RSR}(f_{e,RSR}) \cdot (P_{MPPT} - P_{wind}) \quad \text{(RSR)} & (9) \end{cases}$$

where H is the assigned value of the maximum synthetic inertia to be provided, $\omega_{r,min}$ is the minimum rotor speed, and K_{RSR} (see Fig. 4) is a function of the frequency $f_{e,RSR}$ sampled at the beginning of the RSR operation, defined as

$$K_{RSR}(f_{e,RSR}) = \max\{0, \min\{K_{sat}, K_1 - K_2 f_{e,RSR}\}\} \tag{10}$$

where $K_1 \triangleq \frac{K_{sat} f_{max}}{f_{max} - f_{min}}$, $K_2 \triangleq \frac{K_{sat}}{f_{max} - f_{min}}$ and the meaning of parameters f_{min}, f_{max} and K_{sat} is clarified by Fig. 4. Globally, the VHIE controller depends on 9 parameters: $RoCoF_{act}$, $RoCoF_{deact}$, T_{FS}, ΔP_s, $2H$, $\omega_{r,min}$, K_{sat}, K_1, and K_2.

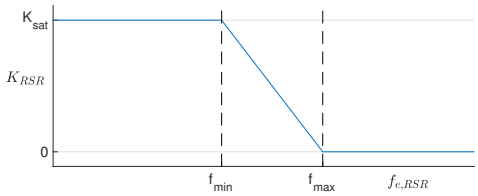


Figure 4: K_{RSR} as a function of $f_{e,RSR}$.

Differently from the standard hidden inertia emulator [23], the inertia constant of the VHIE controller depends on the WTG rotor speed, which allows providing the maximum power contribution at the beginning of the frequency transient by avoiding unstable conditions in case of severe speed reduction. Moreover, the RSR phase is introduced to minimize the secondary frequency drop by setting a proper power reference. All the details about the VHIE controller and its comparisons with alternative state-of-the-art techniques can be found in [20]. It is worth noticing that [20] only considers a Simulink simulated analysis of VHIE, which did not allow taking into account important real-world issues such as, among others, measurement noise and delays, that strongly impact the RoCoF calculation. Frequency measurements obtained by commercial transducers are delayed and subject to

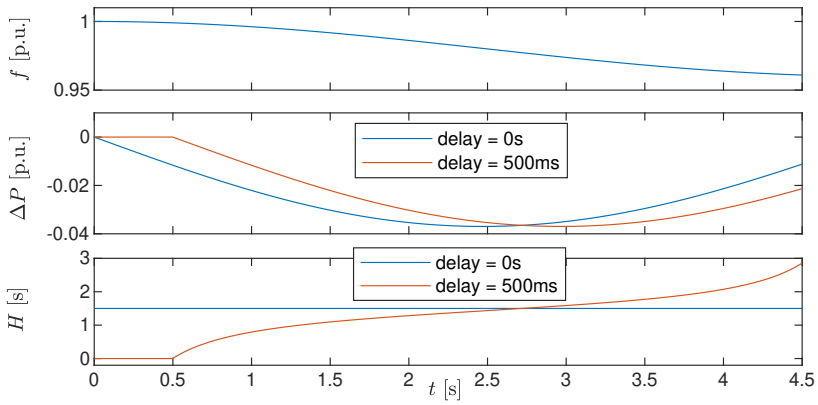


Figure 5: Effect of delays on synthetic inertia production.

noise, then proper filtering is necessary to accurately evaluate the RoCoF, which in turn introduces delay and signal distortions. As an illustrative example, consider the fictitious frequency profile f shown in Fig. 5 (top panel). An ideal synthetic inertia controller would produce a power contribution $\Delta P = 2Hf\frac{df}{dt}$, shown in blue in the middle panel for $H = 1.5$s (blue line in the bottom panel). If the provided power profile were delayed by 500ms (orange curve in the middle panel), the effective inertia, evaluated as $\frac{\Delta P}{2f\frac{df}{dt}}$, would be the orange curve in the bottom panel, which differs from the expected one (in blue). The hardware prototype proposed in this work is a necessary tool for a future investigation of these (and other) effects on the synthetic inertia production and its impact on the grid frequency support.

Table 1 summarizes the effects that are not taken into account in the software (SW) analysis proposed in [20] against the hardware (HW) version proposed in this paper.

3. VHIE controller implementation

A register transfer level description of the VHIE controller is obtained through VHDL (Very High Speed Integrated Circuits Hardware Description Language) code. The block scheme of the digital circuit is shown in Fig. 6. A fixed point representation of data is exploited, where the inputs and outputs are represented with B_{IO} bits, the VHIE parameters (stored in a memory)

Table 1: Effects considered in SW and HW version.

	SW	HW
Measurement noise	no	yes
Freq. meas. delay	no	yes (80ms)
RoCoF FIR filter order N	no	variable
Analog filtering	no	yes
Quantization errors	no	yes
Circuit latency	no	yes (1.12μs)
Sampling interval ΔT	variable (cont. time simul.)	10ms

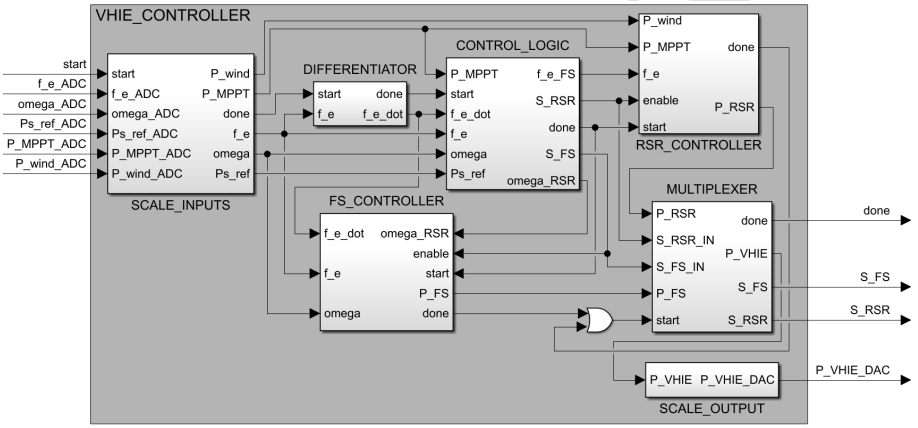


Figure 6: Block scheme of the implemented VHIE controller.

with B bits, and the internal signals have different lengths, depending on the operations they are involved in (e.g., the multiplication between two B-bit values provides a $2B$-bit number), with the only constraints that the multiplications are always performed between B-bit numbers. The point position is also different for each number, such that the minimum number of bits is devoted to representing the integer part of the data, to get maximum precision without overflows, and the remaining bits are used for the decimal part.

All blocks receive in input the clock and the active-low asynchronous reset signals (not shown), and the start signal, activated for one clock cycle indicating that the corresponding block can begin the operation. A common

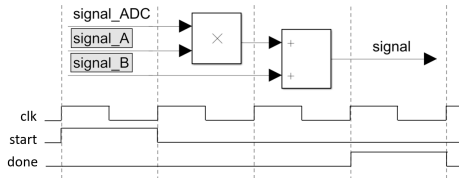


Figure 7: Block scheme of the SCALE_INPUTS block.

output is the done flag, which is also activated for one clock cycle indicating that the operation is concluded and the result is ready. The number of clock cycles between the activation of the start and done signals is the latency of the block.

The inputs of the top module (VHIE_CONTROLLER) are signals f_e_ADC, omega_ADC, Ps_ref_ADC, P_MPPT_ADC, P_wind_ADC representing the controller's inputs provided by an analog-to-digital (ADC) converter. The outputs are P_VHIE_DAC which is the additional power reference to be provided to a digital-to-analog converter (DAC), and flags S_FS and S_RSR, set to 1 if the FS or the RSR phase is active, respectively.

All VHIE parameters as well as the values of B and B_{IO}, are listed in a VHDL package so that they can be easily changed. The architecture is fully parallel to minimize its latency, which is of 4 clock cycles when the controller is inactive, B+10 clock cycles when it operates in FS, and 8 clock cycles when in RSR. Two more clock cycles are necessary during the switch from inactive to FS and from FS to RSR.

In the following subsections the single blocks shown in Fig. 6 are described in detail, with functional block schemes (Figs. 7, 8, 10, 11) indicating which operations are performed within each clock period (delimited by vertical dashed lines) and when signals start and done are active. Also, the parameters stored in the circuit memory are marked as grey rectangles.

3.1. Blocks SCALE_INPUTS, SCALE_OUTPUT

Block SCALE_INPUTS performs a linear scaling of each input, with coefficients $signal\_A$ and $signal\_B$, to convert it from the ADC range $[0,\ 2^{B_{IO}}-1]$ to the correct range:

$$signal = signal\_A \times signal\_ADC + signal\_B \tag{11}$$

where *signal* denotes one of the 5 inputs listed above. Similarly, block SCALE_OUTPUT converts P_VHIE to the DAC range $[0,\ 2^{B_{IO}}-1]$. Each

input is processed in parallel through the circuit shown in Fig. 7, then the SCALE_INPUTS block performs 5 multiplications and 5 sums, whereas the SCALE_OUTPUT block one multiplication and one sum. Both blocks have a latency of 3 clock cycles. The 12 coefficients (10 for the inputs and 2 for the output) of the linear operations are stored in memory.

3.2. Block DIFFERENTIATOR

This block is responsible for evaluating the derivative $\frac{df_e}{dt}\Big|_{t=t_k}$ of the electrical frequency at time t_k, based on N measurements $f_e(t_{k-N+1+n})$ at times $t_{k-N+1+n}$, $n = 0, \ldots, N-1$, with $\Delta T = t_k - t_{k-1}$. The derivative is approximated through the following finite-impulse-response (FIR) filter:

$$\left.\frac{df_e}{dt}\right|_{t=t_k} \approx \sum_{n=0}^{N-1} a_n f_e(t_{k-N+1+n}) \tag{12}$$

where the coefficients a_n only depend on N and the sampling time ΔT, and can be computed offline as

$$a_n = \frac{Nn - \sum_{k=1}^{N-1} k}{\Delta T \left[N \sum_{k=1}^{N-1} k^2 - \left(\sum_{k=1}^{N-1} k \right)^2 \right]}, \quad n = 0, \ldots, N-1 \tag{13}$$

For $N = 2$, Eq. (12) reduces to the standard incremental ratio:

$$\left.\frac{df_e}{dt}\right|_{t=t_k} = \frac{-1}{\Delta T} f_e(t_{k-1}) + \frac{1}{\Delta T} f_e(t_k) \tag{14}$$

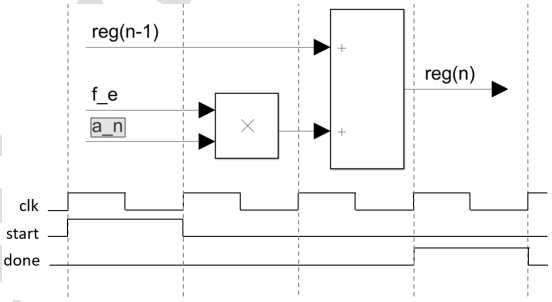


Figure 8: Block scheme of the DIFFERENTIATOR block at time $t_{k-N+1+n}$.

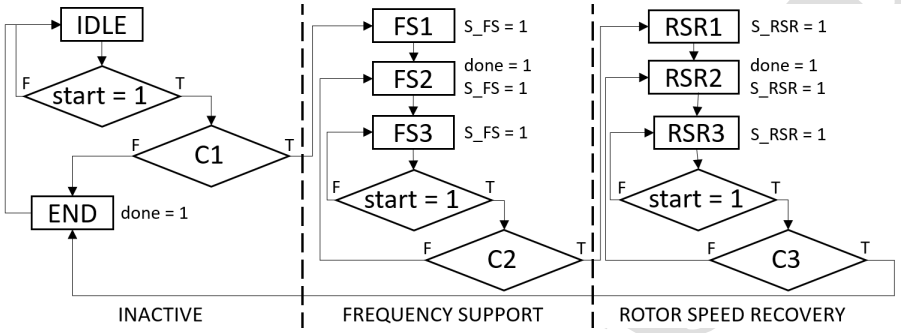


Figure 9: FSM implementing the control logic. The rectangles are the FSM states, whereas the rhombuses indicate the logical conditions. The active flags in each state are indicated on the right side of the rectangles.

The delay of the FIR filter is $\frac{(N-1)\Delta T}{2}$, then N should be chosen as small as possible. Nevertheless, low values of N make the estimation very sensitive to measurement noise and then inaccurate. A trade-off is therefore necessary. At time $t_{k-N+1+n}$, the block performs the operations shown in Fig. 8, by storing in a register reg(n) the content of register reg(n-1) plus term $a_n f_e(t_{k-N+1+n})$, where register reg(-1) (for $n = 0$) contains 0. The latency of the block is 3 clock cycles. The content of register reg(n) converges to $\frac{df_e}{dt}\big|_{t=t_k}$ (signal f_e_dot) as n increases.

3.3. Block CONTROL_LOGIC

This block is responsible for activating/deactivating the FS and RSR modes of the controller. It is implemented as the finite state machine (FSM) shown in Fig. 9, where C1, C2, and C3 represent logical conditions (4), (5) and (6), respectively. When the reset signal is set to 1, the FSM goes in state IDLE. States FS1, FS2, FS3 correspond to the frequency support operation, whereas states RSR1, RSR2, RSR3 to the rotor speed recovery phase. At the end of the operation, the END state is reached and then the FSM comes back to the IDLE state. The labels in the right side of the rectangles in Fig. 9 denote the active flags in the corresponding state. The maximum latency of this block is 2 clock cycles, corresponding to the switch from inactive to FS or from FS to RSR.

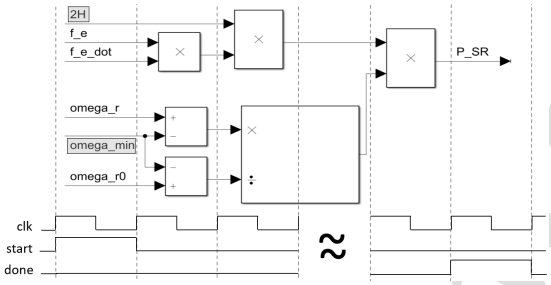


Figure 10: Block scheme of the FS_controller block.

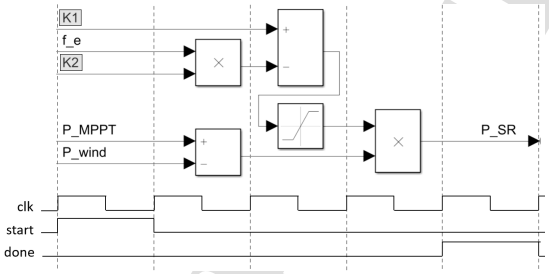


Figure 11: Block scheme of the RSR_controller block.

3.4. Blocks FS_CONTROLLER and RSR_CONTROLLER

Block FS_CONTROLLER (see Fig. 10) implements Eq. (8), whose coefficients $2H$ and $\omega_{r,min}$ are stored in memory. A *non-restoring division* algorithm [24] is exploited to evaluate the ratio between $\omega_r - \omega_{r,min}$ and $\omega_{r,min} - \omega_{r,FS}$. The latency of this operation is $B + 2$ clock cycles, then the total latency of the block is $B + 6$ clock cycles.

Block RSR_CONTROLLER (see Fig. 11) implements Eq. (9). Coefficients K_1 and K_2 are stored in memory. The whole latency is 4 clock cycles.

These two blocks perform the operations only if input enable is active; otherwise, the signal done is activated immediately after the start command and P_FS or P_RSR are set to 0.

3.5. Block MULTIPLEXER

When either the FS_CONTROLLER or the RSR_CONTROLLER activate the done signal, this block checks flags S_FS and S_RSR provided by the control logic, indicating the current mode of the controller. If the controller

is inactive (both flags are 0) the output P_VHIE is set to 0, otherwise, it is set to either P_FS (provided by the FS_CONTROLLER) or P_RSR (provided by the RSR_CONTROLLER). The operation is performed in one clock cycle.

4. VHIE controller prototype

The implemented hardware prototype, whose picture and functional block scheme are shown in Fig. 12, is composed of:

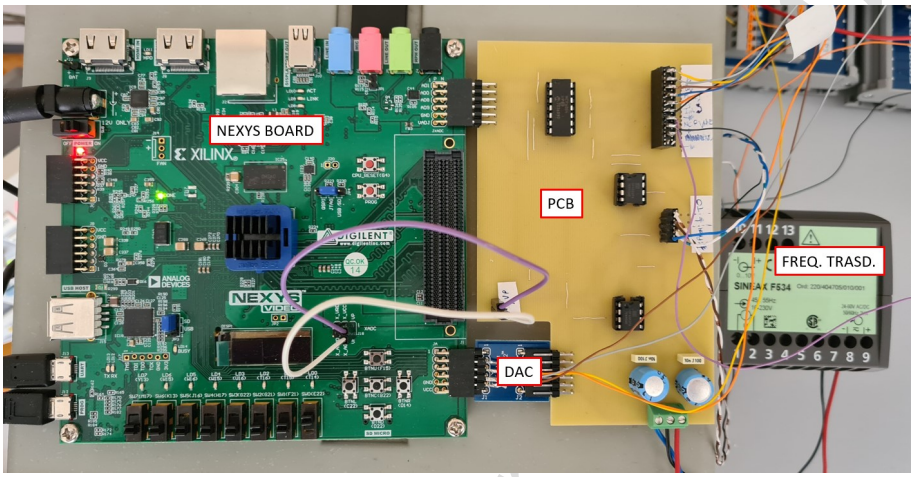
- a Digilent Nexys Video Artix-7 FPGA board, which embeds the VHIE controller and an ADC activated by a timer;
- a Digilent PmodDA2 board equipped with a DAC;
- a frequency transducer SINEAX F534, to sense the frequency of the periodic voltage measured at the converters' output;
- PCB necessary to interface the FPGA board and the frequency transducer to either the real wind power system or, as in this case, a real-time simulator (as detailed in Sec. 5.1).

4.1. NEXYS board and DAC

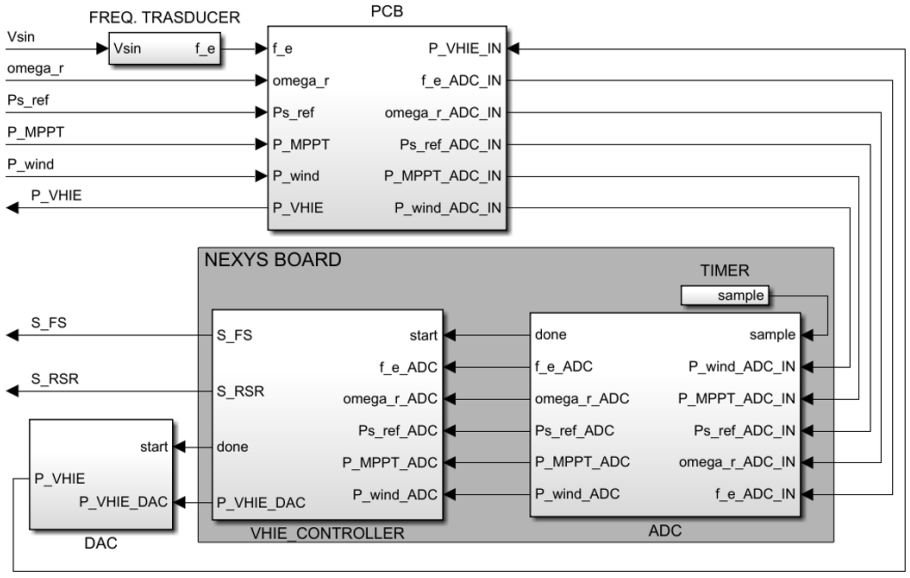
A Digilent Nexys Video board is exploited to implement the VHIE controller. The board is equipped with a Xilinx Artix-7 XC7A200T-1SBG484C FPGA, with 33650 logic slices, 740 DSP slices, and an on-chip 12-bit ADC with 16 channels, 5 of which are connected to a PMOD interface, and an input range of [0 1]V. Each DSP slice comprises a 25×18 bit two's complement multiplier and a 48-bit accumulator. Due to these hardware specifications, we set $B = 18$ and $B_{IO} = 12$ for the VHIE controller.

A timer provides a sample signal to the ADC every ΔT, to acquire the five inputs. As soon as measurements are ready, the ADC activates the done signal, which corresponds to the start signal of the VHIE_CONTROLLER block. The latency (from sample to done) of the ADC is 84 clock cycles, therefore the whole circuit maximum latency is 112 clock cycles, which corresponds to 1.12 μs, being the FPGA clock frequency of 100 MHz.

The Nexys board does not include DACs, therefore an external board (Digilent Pmod DA2) equipped with 2 12-bit DACs, is connected to the main board through the PMOD interface. One DAC is used to convert the VHIE controller output P_{VHIE} from a 12-bit digital representation to an analog voltage in the range [0 3.3] V.



(a)



(b)

Figure 12: Picture (a) and block scheme (b) of the realized VHIE controller prototype.

4.2. Frequency transducer

The electrical frequency measurement represents a fundamental aspect of the prototype development. Inertial support requires a very fast activation, in the order of magnitude of hundreds of milliseconds, as the contribution to limiting the initial RoCoF is effective only if provided in the very first moments of the transient, otherwise, the support action requested from the auxiliary controller can be nullified. From market analysis, it was possible to identify a very performing frequency sensor, the SINEAX F534 manufactured by Camille Bauer, that allows obtaining a frequency measurement with a response time of only 2 cycles (i.e., 40 ms in the case of 50 Hz systems). This sensor can measure the fundamental frequency of either a sinusoidal or square waveform, even in the presence of significant harmonic distortion. The measurement range goes from 45 Hz to 55 Hz for voltage waveforms with root mean square value comprised between 10 V and 690 V. The frequency measurement is provided as an analog voltage ranging from 0 V (45 Hz) to 10 V (55 Hz). The supply voltage can be provided either by the input periodic signal if its power is sufficient, or by an external power supply, as a constant 30 V voltage, as in this case.

4.3. PCB

A PCB is necessary to interface the Nexys board to the frequency transducer and either the real power grid or, as in this case, to a real-time simulator. The PCB only performs signal conditioning and filtering, therefore, it can be easily re-designed in the case the VHIE prototype should be connected to a real wind power system. The PCB is equipped with 5 connectors: two PMOD interfaces to the Nexys board and DAC, two pin header connectors to the simulator and the frequency transducer, and a 3-pin connector to the supply voltage ($\pm 30V$, GND).

The considered simulator (described in Sec. 5.1) provides to the PCB the periodical voltage at the output of the GSC in a range [-5 5] V, which is amplified with a gain of 5.7 through the circuit shown in Fig. 13 (a), exploiting a Texas Instruments OPA552 operational amplifier. The amplified signal, in the range [-28.5 28.5] V, has a root mean square value of about 20 V, compatible with the frequency transducer, and then is provided to the SINEAX F534 together with supply voltages GND and +30 V. The transducer returns to the PCB the frequency signal f_e in a range [0 10] V. The other inputs of the VHIE controller (ω_r, P_{ref}, P_{MPPT}, P_{wind}) are provided by the simulator with ranges [0 10] V. These five signals are filtered with a

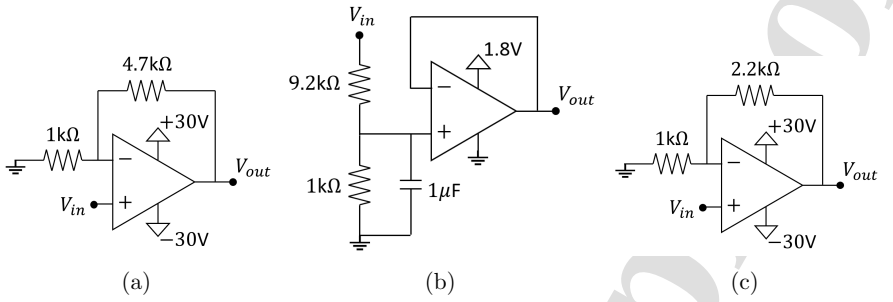


Figure 13: Analog amplifiers exploited in the PCB.

first-order low-pass filter with a cutoff frequency of 180Hz and attenuated 10 times through 5 copies of the circuit shown in Fig. 13 (b), exploiting a Microchip Technology MCP600x operational amplifier. The supply voltage of 1.8V is provided directly by the Nexys board. The resulting signals, in the range [0 1] V, are provided to the Nexys board and acquired by the ADC.

The DAC provides to the PCB signal P_{VHIE} in a range [0 3.3] V, which is amplified with gain 3.2 by the circuit shown in Fig. 13 (c), exploiting the OPA552 amplifier, and provided to the simulator in a range of approximately [0 10] V.

5. Experimental setup and results

The experimental setup used to validate the proposed VHIE controller prototype is shown in Fig. 14. The VHIE prototype is connected to the real-time simulator SpeedGoat implementing the power system model, and a power supply is used to provide the ±30 V and reference (0 V) voltages to the PCB.

5.1. SpeedGoat real-time simulator

SpeedGoat is a high-performance real-time simulator that allows running models developed in the Simulink/Simscape environment in real-time, by exploiting its embedded INTEL Core CPUs and FPGAs. SpeedGoat is provided with several analog and digital input/output interfaces to easily connect external devices, e.g., the proposed VHIE prototype, to perform hardware-in-the-loop simulations. The analog signals provided by SpeedGoat are quite noisy, as visible in Fig. 15, where the profile of ω_r imposed in

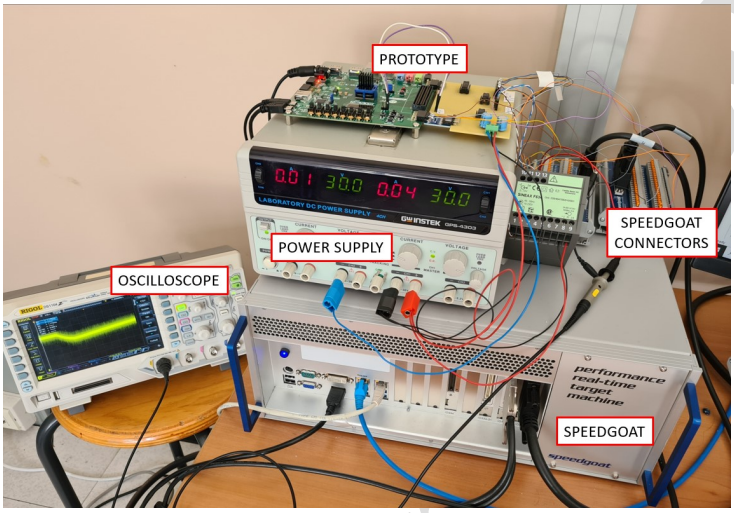


Figure 14: Picture of the experimental setup.

Simulink and measured at the SpeedGoat output are shown in orange and blue, respectively. This makes the filtering process performed by the PCB necessary to make the prototype work properly.

In this work, hardware-in-the-loop simulations are carried out, where the VHIE prototype is connected (through analog interfaces) to SpeedGoat, running in real-time the power system model shown in Fig. 16 with its main controllers, developed by exploiting Simscape blocks. The main model parameters are listed in Tab. 2.

A 2 MVA permanent magnet synchronous generator, whose active power P_s depends on the imposed wind speed v_w, is connected to the MSC through a cable, modeled by a resistance R_c and an inductance L_c, and a filter, whose longitudinal branch has resistance R_{fc} and inductance L_{fc} and the transverse branch is neglected, as only the first harmonic of voltages and currents is considered. The MSC is interfaced to the GSC through a DC-link with capacitance C_{dc}. The output voltage of the conversion stage is smoothed by a filter with resistance R_{fg} and inductance L_{fg} (only longitudinal branch) and raised from 0.69 kV to 20 kV through a LV/MV transformer, to be compatible with the wind farm distribution. Finally, the connection to the high-voltage grid is realized through a medium voltage cable, modeled with resistance R_g and inductance L_g, and an MV/HV park step-up transformer from 20 kV to

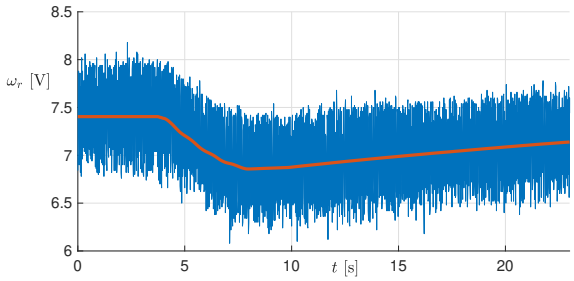


Figure 15: Nominal profile of ω_r imposed in Simulink (orange) and measured SpeedGoat output (blue).

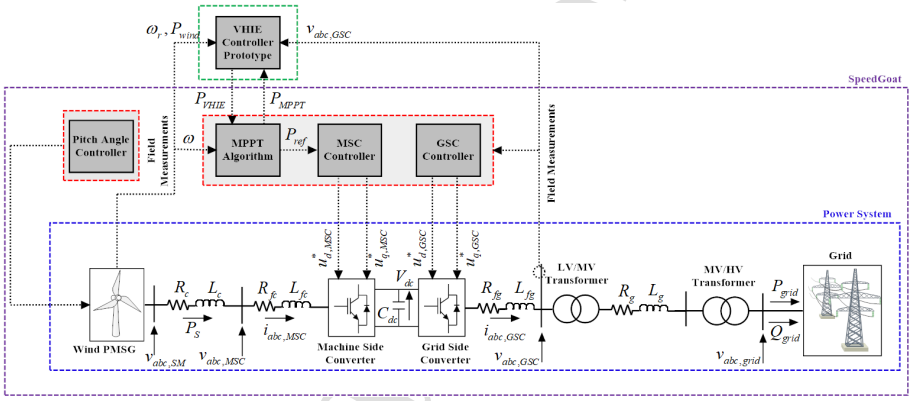


Figure 16: Detailed scheme of the wind generator, with its main controllers and the additional VHIE controller.

150 kV. The LV/MV (MV/HV) transformer has a rated power of 2.5 (50) MVA, a percent short circuit voltage of 6% (12%), and a no-load power of 1.1 (14) kW. The high-voltage grid is modeled as a frequency-dependent voltage source, with an imposed frequency profile f_e. The detailed model of the high-voltage grid is not implemented in the SpeedGoat simulator, because this would require computational resources that cannot guarantee that the simulation runs in real-time. Then, the open-loop approach is applied in this context, in which the frequency profile is imposed to trigger the activation of the prototype.

The MSC is controlled with a Pulse Width Modulation (PWM) technique

Parameter	Value	Parameter	Value
R_c	2.4 mΩ	L_c	5 mH
R_{fc}	0.01 Ω	L_{fc}	0.3 mH
R_{fg}	0.02 Ω	L_{fg}	0.15 mH
R_g	0.1 Ω	L_g	0.6 mH
C_{dc}	30 mF		

Table 2: Parameters of the power system implemented in SpeedGoat.

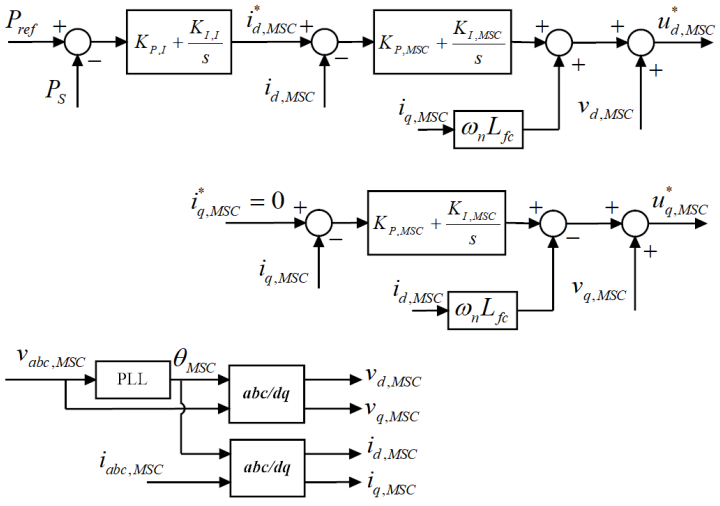


Figure 17: MSC control scheme.

whose modulating signals, expressed in the rotating reference system dq, are $u^*_{d,MSC}$ and $u^*_{q,MSC}$. These signals are provided through a classical control architecture (Fig. 17), such that the PMSG active power P_s is regulated to its reference value P_{ref}. The direct and quadrature voltages $(v_{d,MSC}, v_{q,MSC})$ and currents $(i_{d,MSC}, i_{q,MSC})$ are obtained based on measurements of the three-phase voltages $v_{abc,MSC}$ and currents $i_{abc,MSC}$ (see Fig. 16). A Phase-Locked-Loop (PLL) is exploited to obtain the angle θ_{MSC} aligned to voltage $v_{abc,MSC}$ (see Fig. 17, bottom part).

The GSC performs a DC/AC voltage conversion and is also controlled with PWM, whose modulating signals are $u^*_{d,GSC}$ and $u^*_{q,GSC}$ (see Fig. 18). The GSC is used to both regulate the DC-link voltage V_{dc} to its reference

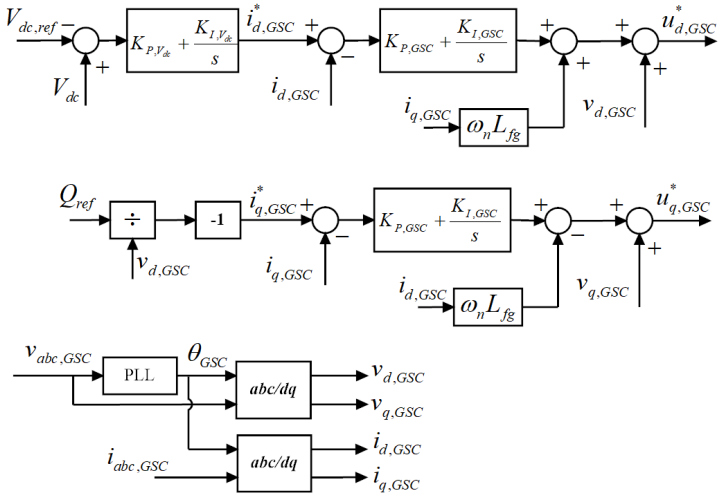


Figure 18: GSC control scheme.

value $V_{dc,ref}$ and maintain its output reactive power at the reference value Q_{ref}. The MSC and GSC controllers parameters are listed in Tab. 3.

The MPPT power, in p.u., is evaluated through Eq. (2), with $\omega_{r,cutin} = 0.5$ p.u., $\omega_{r,min} = 0$ p.u., $\omega_{r,max} = 1.2$ p.u., and $P_{max} = 1$ p.u., whereas the wind power is evaluated through Eq. (3), with $\rho = 1.19$ kg/m^3, $R = 40$ m, $A_r = \pi R^2$, $\omega_{r,n} = 2.36$ rad/s, and $P_n = 2$ MVA. Function C_p is the same shown in [22].

The implemented pitch controller (Fig. 19) is a PI regulator operating on the servomotor that imposes the blades' pitch angle β. The servomotor is modeled as an integrator with a time constant T_P, when the rotor speed

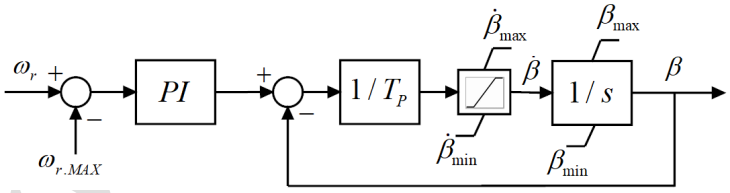


Figure 19: Pitch angle controller implementation.

Parameter	Value	Parameter	Value
$K_{P,I}$	0.0001 V/A	$K_{I,I}$	0.03 V/As
$K_{P,MSC}$	0.009 A/W	$K_{I,MSC}$	1 A/Ws
$K_{P,V_{dc}}$	3 A/V	$K_{P,V_{dc}}$	8 A/Vs
$K_{P,GSC}$	0.1 V/A	$K_{I,GSC}$	1 V/As

Table 3: MSC and GSC controllers parameters.

exceeds the value $\omega_{r,MAX}$ equal to 1.2 p.u. The pitch angle is limited between $\beta_{min} = 0°$ and $\beta_{max} = 27°$ and its derivative is limited between $\dot{\beta}_{min} = -10°/s$ and $\dot{\beta}_{max} = 10°/s$.

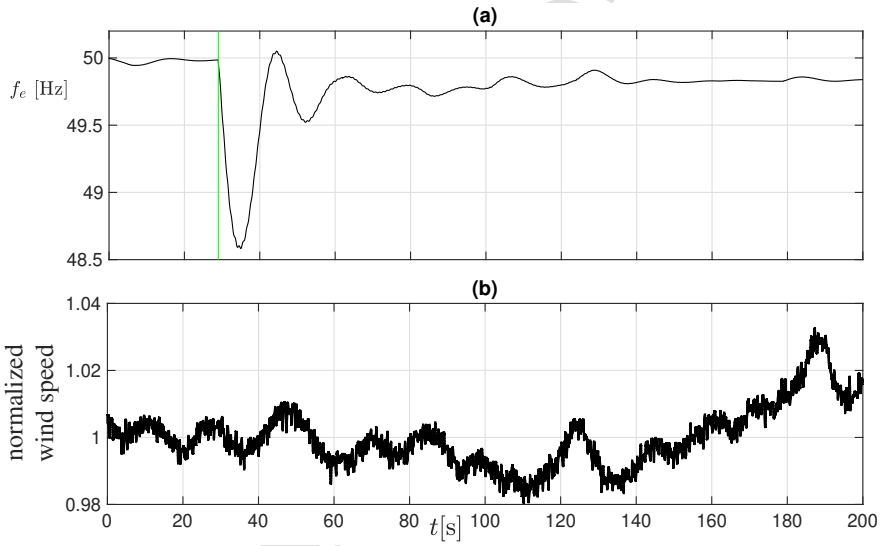


Figure 20: (a) Frequency profile generated by DIgSILENT PowerFactory ®and (b) normalized wind speed profile used for real-time simulations.

The simulation model requires two input functions, namely, the frequency profile $f_e(t)$ and the wind speed profile $v_w(t)$. The former is obtained by simulating a realistic test power grid with low inertia through DIgSILENT PowerFactory®. This tool allows for accurately modeling and simulating the main components of an electrical transmission system, to obtain the

voltage and frequency dynamics. The resulting frequency profile is shown in Fig. 20 (a): at $t = 29$ s a perturbation in the grid occurs, causing marked frequency oscillations, owing to the low grid inertia. This frequency profile is used to drive the voltage source in the SpeedGoat model representing the high-voltage grid.

Concerning the wind speed profile, the normalized measured wind speed profile $v_{wn}(t)$ shown in Fig. 20 (b) is used for the wind tower of the SpeedGoat model. The used wind speed profile $v_w(t)$ is obtained by multiplying the normalized profile by the average wind speed $\overline{v}_w$, i.e., $v_w(t) = \overline{v}_w v_{wn}(t)$, being $\overline{v}_w$ the actual simulation input. This approach is used to simulate scenarios with different levels of wind speed, corresponding to different scenarios of power production.

5.2. Preliminary tests

A set of preliminary simulations in different scenarios are performed where the VHIE controller is implemented in SpeedGoat with floating-point double precision, by neglecting measurement noise and the delay of the frequency transducer. These simulations aim to define the sampling interval and the variation range of the signals before hardware-in-the-loop tests. Satisfactory results are obtained by performing the real-time simulation in discrete time with a sampling time of 50μs. The MSC and the GSC controller inputs are acquired with a sampling time of 100μs, whereas the signals provided to the VHIE controller are updated every $\Delta T = 10$ ms. Then, also the additional power P_{VHIE} is provided to SpeedGoat by the prototype every 10 ms. Simulation results showed that the signals in input/output to the VHIE controller vary in the ranges listed in Tab. 4. Then the coefficients signal_A and signal_B of blocks SCALE_INPUTS and SCALE_OUTPUTS (also listed in the table) are set so that the ranges correspond to interval [0 4095], imposed by the choice of $B_{IO} = 12$.

A further test has been performed to identify the order N of the FIR filter exploited to compute the RoCoF. To this aim, the sinusoidal voltage $v_{a,GSC}$ is acquired with the frequency transducer. Figure 21 (a) shows the reference (blue) and measured (orange) unfiltered frequency of the voltage signal for $t \in [28\ 80]$ s. One can notice the presence of some measurement noise and a delay, introduced by the transducer, of approximately 80 ms. Both signals are sampled with an interval $\Delta T = 10$ ms. Figure 21 (b) shows the RoCoF of the reference frequency profile (blue curve) estimated through Eq. (12) with $N = 2$, as the nominal frequency is not corrupted by noise. Equation

signal	range [p.u.]	signal_A	signal_B
f_e	[0.9 1.1]	$4.88 \cdot 10^{-5}$	0.9
omega	[0 1.2]	$2.93 \cdot 10^{-4}$	0
Ps_ref	[0 1.2]	$2.93 \cdot 10^{-4}$	0
P_MPPT	[0 1.2]	$2.93 \cdot 10^{-4}$	0
P_wind	[0 1.5]	$3.66 \cdot 10^{-4}$	0
P_VHIE	[0 1.2]	3412.5	0

Table 4: Ranges and parameters for the linear scalings.

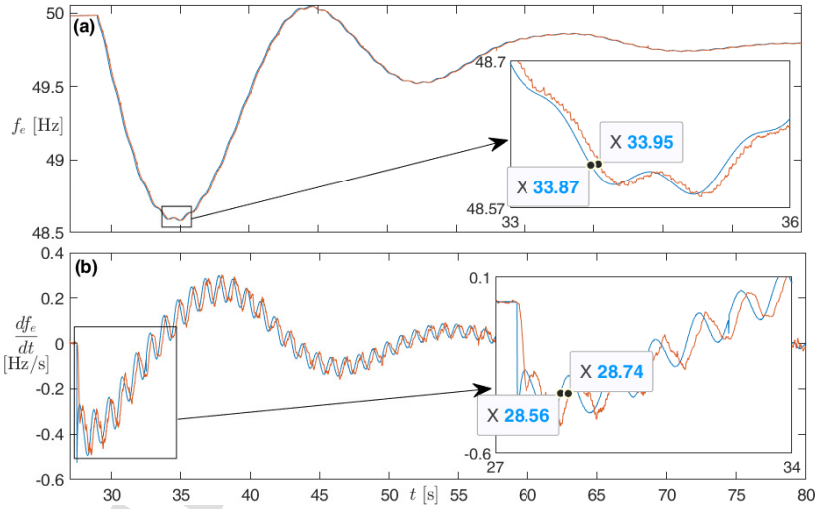


Figure 21: (a): reference (blue) and measured (orange) frequency; (b): reference (blue) and estimated (orange) RoCoF.

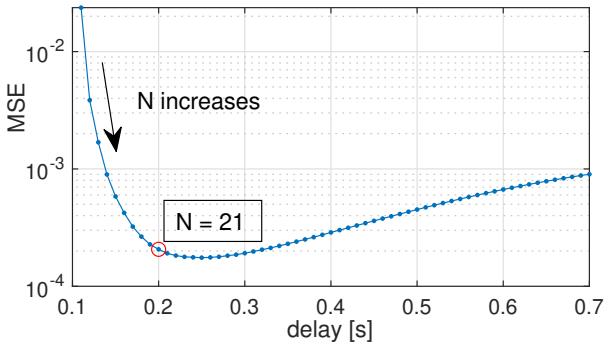


Figure 22: Error vs delay in RoCoF estimation for different values of N.

(12) has been then used, for different values of N, on the noisy frequency signal measured by the transducer. The resulting RoCoF[1] has been aligned with the reference signal, by compensating both the transducer and filtering delays, and the root mean square error (RMSE) between these signals has been evaluated for different values of N. A plot of the error versus the total delay is shown in Fig. 22, being the total delay equal to the transducer delay (80ms) plus the filtering delay $\frac{N}{2}\Delta T$. As expected, increasing N (see black arrow) leads to an increase in the delay, with a decrease in the error. However, if N is too large, the error increases again as the filtering is too strong and some oscillations of the frequency signal are attenuated. The minimum RMSE is obtained for $N = 31$, however, for $N > 21$ the error decreases of a very small amount, at the cost of a higher delay. Then, in this work, we chose $N = 21$ as a good compromise between estimation accuracy and delay (180 ms). The resulting estimated RoCoF of the noisy measured frequency is the orange curve in Fig. 21 (b). Notice also the low-pass filter effect, particularly visible when the RoCoF suddenly drops, as the slope of the orange curve is lower than that of the blue curve (see, in particular, the inset in the figure). Since the FS mode is activated when the RoCoF goes below threshold $RoCoF_{act}$, the delay in FS activation will be lower than 180ms (see next section).

[1]The estimation has been performed in MATLAB with floating-point double precision. The effect of quantization and rounding errors are not included.

Parameter	Value	Parameter	Value
$RoCoF_{act}$	-0.005 p.u./s	K_{sat}	0.9
$RoCoF_{deact}$	0.02 p.u./s	$\omega_{r,min}$	0.2 p.u.
f_{min}	0.96 p.u.	ΔP	0.04 p.u.
f_{max}	0.996 p.u.	T_{FS}	∞
K_1	24.9	K_2	25

Table 5: VHIE controller parameters.

5.3. Hardware-in-the-loop simulations results

Hardware-in-the-loop simulations, with the VHIE prototype connected to SpeedGoat, have been performed to assess the functionality of the proposed hardware realization. For comparison purposes, the VHIE controller is also implemented in SpeedGoat (in open-loop), so that the effects of delays and measurement noise of the proposed prototype can be evaluated compared to the reference controller proposed in [20]. Closed-loop simulation results can be found in [20]. Also in the Simulink twin, the RoCoF is computed with the same FIR filter with $N = 21$ implemented in the prototype. Three different scenarios have been considered: *test 1*, *test 2* and *test 3*. In *test 1* the controller provides a high value of virtual inertia in a low wind speed condition, by avoiding the turbine stall; in *test 2* the VHIE controller prototype provides a low value of virtual inertia with a medium wind speed, whereas in *test 3* the VHIE controller prototype operates when the pitch angle regulator controls the blade angles to limit the rotor speed. All VHIE controller parameters, excluding H, are fixed for all scenarios and are listed in Tab. 5.

5.3.1. Test 1

The first simulation is with $H = 35$ s and the average wind speed $\overline{v}_w = 9.7$ m/s. The results are shown in Fig. 23. Panel (a) shows the output $P_{VHIE,HW}$ of the VHIE prototype (blue curve) and $P_{VHIE,SW}$ of the VHIE controller implemented in Simulink (red curve). Notice the presence of oscillations on the blue signal due to both measurement noise and the quantization mainly of the ADC and DAC. Also, the signal is delayed by about 90 ms compared to the red curve, owing to the frequency transducer (not modeled in Simulink), as better highlighted in the enlargement of Fig. 24.

The RMSE and maximum absolute error between $P_{VHIE,SW}$ delayed of 90 ms and $P_{VHIE,HW}$ are 45.6 kW and 152 kW, respectively. The normalized

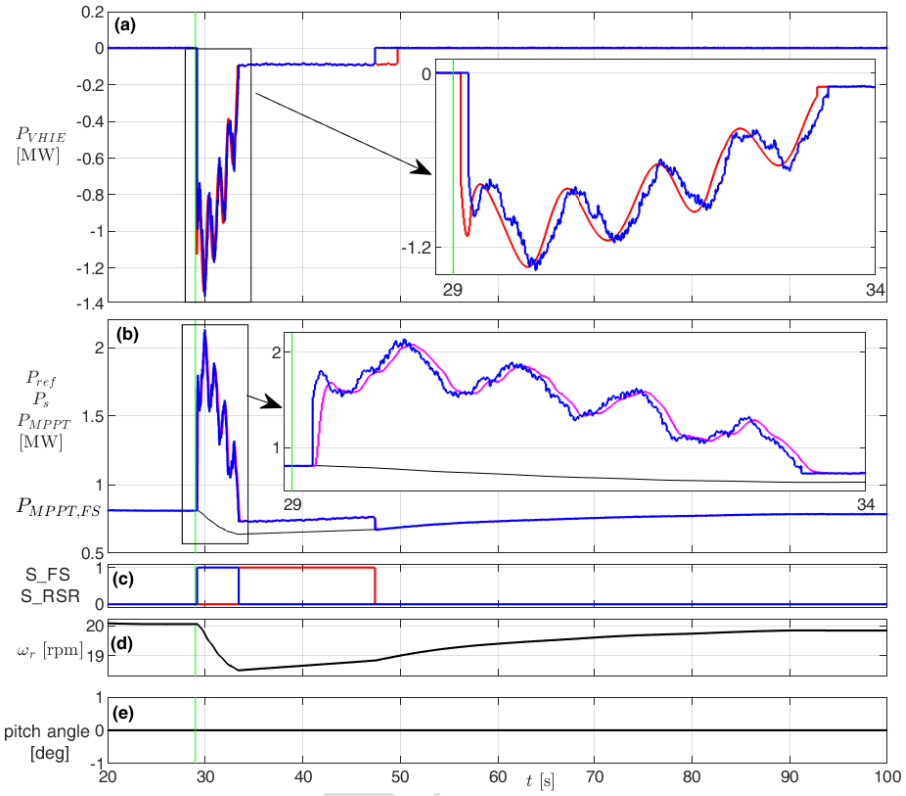


Figure 23: Results of *test 1*. (a) P_{VHIE} provided by the prototype (blue) and by Simulink (red); (b) P_{ref} (blue), P_s (magenta), and P_{MPPT} (black); (c) signals S_FS (blue) and S_RSR (red) provided by the prototype; (d) ω_r; (e) pitch angle. The vertical green line denotes the instant where the perturbation occurs.

errors with respect to the maximum absolute value of $P_{VHIE,SW}$ (about 1.34 MW) are 3.4% and 11.3 %.

Figure 23 (b) shows the time evolution of P_{MPPT} (black), P_{ref} (blue) and P_s (magenta), whereas panel (c) shows signals S_FS and S_RSR indicating the controller mode. For $t < 29$ s the system is at steady state, then the controller is inactive ($P_{VHIE} = 0$), and both P_s and its reference value P_{ref} coincide with P_{MPPT}. At $t = 29$ s the frequency suddenly drops (see Fig. 20 (a)) and the controller prototype enters the FS mode after 180 ms. The extra

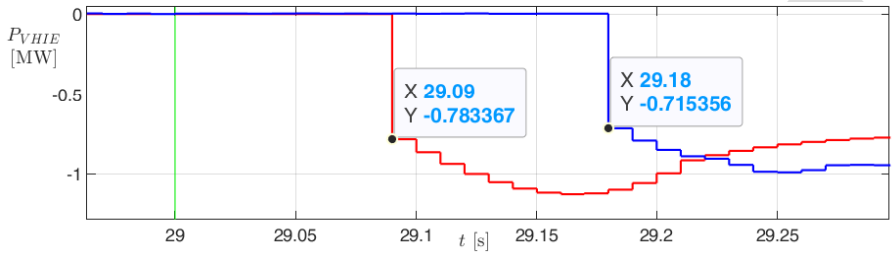


Figure 24: Detail of the comparison between P_{VHIE} provided by the prototype (blue) and by Simulink (red).

power reference P_{VHIE}, with a maximum absolute value of about 1.34 MW, causes P_{ref} (and then P_s) to increase above the MPPT point. This implies that the rotor speed (panel (d)), and then P_{MPPT}, significantly decrease due to the high imposed virtual inertia H. After about 4 s, the condition $P_{ref} \leq P_{MPPT,FS}$ is verified, then the RSR operation starts, lasting about 14 s. In this phase, the reference power is slightly greater than P_{MPPT} and the rotor speed starts increasing. The speed increases faster when the RSR operation ends and the controller becomes inactive again, with $P_{ref} = P_{MPPT}$.

Notice that the controller prototype exits the RSR operation, see panel (a), two seconds earlier than the Simulink controller, due to the measurement noise that triggers the output condition. However, this difference does not compromise the correct functioning of the system.

5.3.2. Test 2

The second simulation is with $H = 5$ s and with the average wind speed equal to 12.2 m/s. The results are shown in Fig. 25. As one can see from panel (a) the inertial power contribution during FS, reaching about 190kW, is reduced compared to *test 1*. Consequently, the rotor speed deceleration is reduced, as shown in panel (d), then the RSR phase is not activated in this scenario.

The RMSE and maximum absolute error between $P_{VHIE,SW}$ delayed of 90 ms and $P_{VHIE,HW}$ are 7.4 kW and 33.9 kW, respectively. The normalized errors with respect to the maximum absolute value of $P_{VHIE,SW}$ (about 190 kW) are 3.8% and 17.8 %.

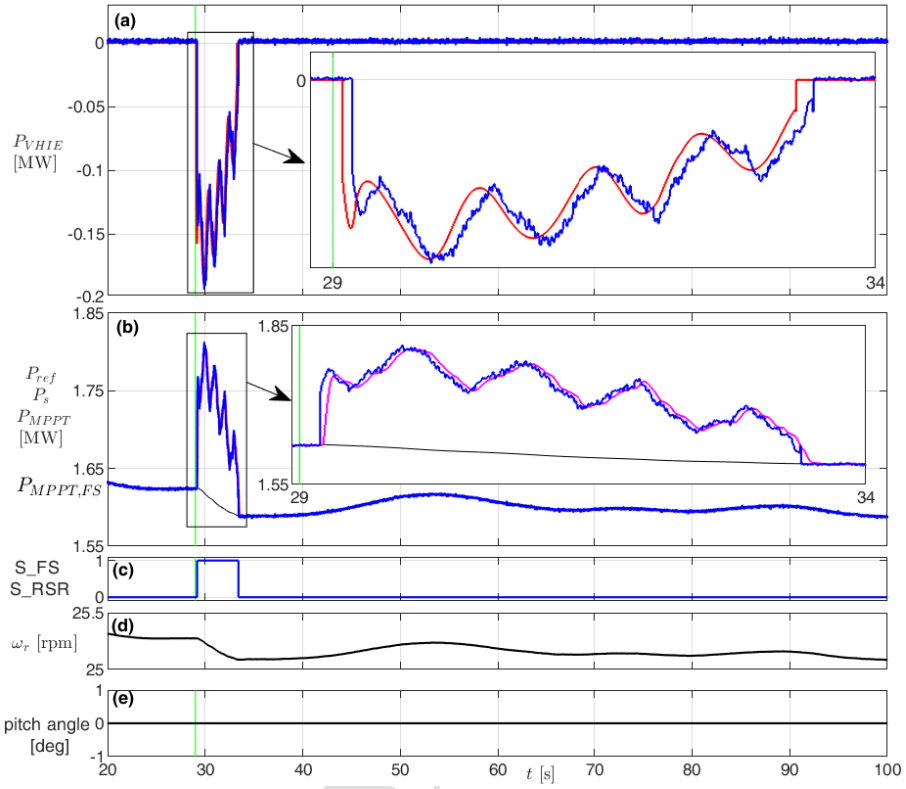


Figure 25: Results of *test 2*. (a) P_{VHIE} provided by the prototype (blue) and by Simulink (red); (b) P_{ref} (blue), P_s (magenta) and P_{MPPT} (black); (c) signals S_FS (blue) and S_RSR (red) provided by the prototype; (d) ω_r; (e) pitch angle. The vertical green line denotes the instant where the perturbation occurs.

5.3.3. Test 3

The third simulation is again with $H = 35s$ and with the wind speed equal to 13.2 m/s, thus implying the action of the pitch angle controller. The results are shown in Fig. 26. As visible in panel (a), the inertial active power contribution is almost the same as *test 1*, but the initial value of P_{MPPT}, panel (b), is higher, being dependent on the wind speed. This leads to the saturation of P_{ref}, set to 2.4 MW. The deceleration of the wind turbine rotor, panel (d), during the FS phase causes a reduction of the pitch angle,

as shown in panel (e), which in turn controls the rotor speed. Due to the pitch controller, the rotor deceleration is small, thus not requiring the RSR phase.

The RMSE and maximum absolute error between $P_{VHIE,SW}$ delayed of 90 ms and $P_{VHIE,HW}$ are 43.9 kW and 186 kW, respectively. The normalized errors with respect to the maximum absolute value of $P_{VHIE,SW}$ (about 1.35 MW) are 3.3% and 13.7 %.

We remark that, as the controller works in p.u., the relative errors in the three considered tests are comparable.

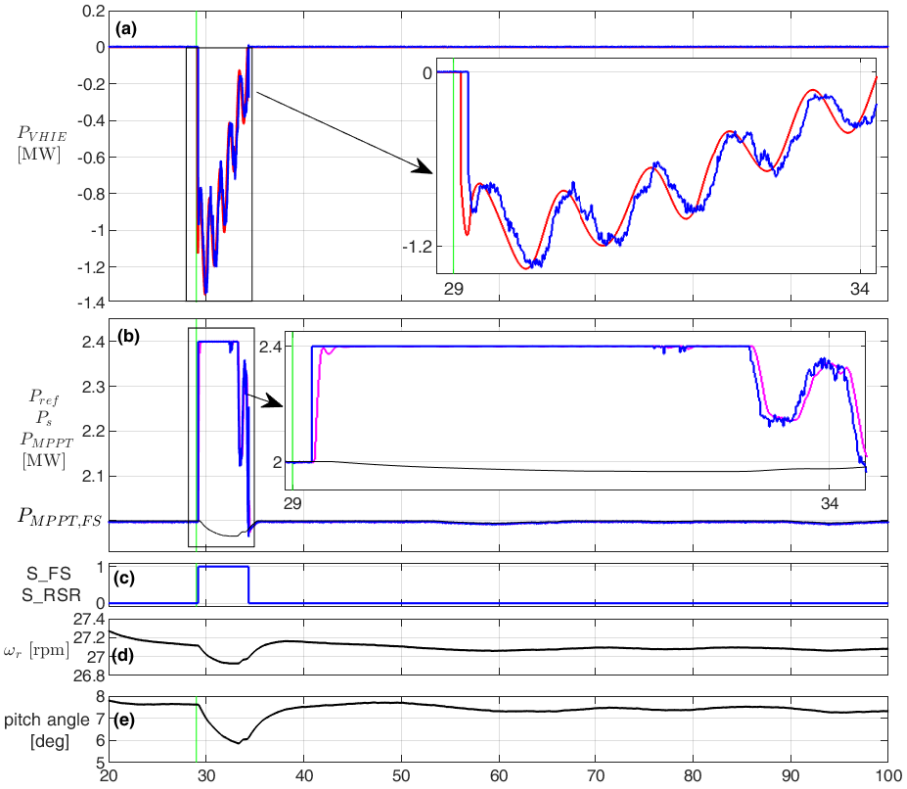


Figure 26: Results of *test 3*. (a) P_{VHIE} provided by the prototype (blue) and by Simulink (red); (b) P_{ref} (blue), P_s (magenta) and P_{MPPT} (black); (c) signals S_FS (blue) and S_RSR (red) provided by the prototype; (d) ω_r; (e) pitch angle. The vertical green line denotes the instant where the perturbation occurs.

6. Conclusions

This work proposed the hardware prototype of the innovative VHIE synthetic inertia controller for WTGs. The embedded realization of the controller allowed for overcoming implementation issues and evaluating real-world effects on the VHIE performances. In the first part of the paper, all the elements necessary for the real deployment of the VHIE controller have been presented, leading to the final design of the hardware prototype. The prototype is composed of an FPGA board, a frequency transducer, and a printed circuit board, useful to easily interface the prototype to different devices (e.g., a real-time simulator or a real WTG inverter). The hardware prototype was tested through HIL simulations, where a model of a grid-connected WTG was implemented in the Speedgoat real-time simulator. The correct functionality of the prototype and some real-world effects such as measurement noise, delays, quantization errors, latency, and filtering distortions have been assessed in three different scenarios, leading to a delay of 90 ms in the controller output, compared to the ideal simulation, with RMSE and maximum relative errors below 4% and 18% in all considered cases. The embedded digital controller has a latency of about 1μs, which is negligible compared to the sampling interval of the measurements (10 ms). The results are quite satisfactory from an applicative point of view and contribute to an advancement in the effective deployment of innovative synthetic inertia controllers in a real application. The main limitations of the present work consist in the open-loop operation of the prototype and in the limited modeling of mechanical phenomena on the WTG rotor shaft. However, feedback from this analysis will allow for increasing the performance of the prototype (e.g., in terms of activation delay) and assessing the effectiveness of a realistic inertial response on a power system. Future development shall include the possibility of using a more performing real-time simulator, able to perform a closed-loop simulation with a realistic model of the power grid. Moreover, this will allow including a mechanical modeling of the wind turbine. These are necessary steps to take the prototype to an industrial stage, to be tested on a real wind turbine, being compliant with grid code requirements for inertial frequency support.

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Declaration of interests

☐ The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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